Power Management for Neural Signal Acquisition IC

Andreas Hammer

School of Electrical Engineering

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Thesis supervisor:

Prof. Jussi Ryynänen

Thesis advisor:

D.Sc. (Tech.) Marko Kosunen

Aalto University
School of Electrical
Engineering

AALTO UNIVERSITY
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Advisor: D.Sc. (Tech.) Marko Kosunen

Wireless biosignal measurement is a growing opportunity to increase the efficiency of medical procedures: An integrated circuit (receiver) is implanted inside human tissue and it's output can be read wirelessly with a transmitter that also provides energy for the implant. This method requires RFID technology, where wireless data is transmitted in the RF-band back-and-forth between the receiver and transmitter. The receiver can be implemented either as an active design, where a local power supply is required inside the receiver, or as a passive design without internal energy storage. However, as the modern CMOS process is fairly advanced and the power consumption is low - passive designs are the most common.
In the passive design the power for the receiver is drawn from the electromagnetic field transmitted to the chip, generally with electromagnetic induction. A design and implementation of an 860 MHz UHF-band RFID power system is presented in this work and its performance evaluated. The system was designed for a wireless EEG (electroencephalography) reader that can be implanted under the skalp - but the design principles can be expanded upon any RF-band RFID system.
The final system works with an input power of -6.8 dBm with a startup time of slightly below 40 μs with specifications of 700 mV to 150 μA load. The LDO line regulation achieves a -51 dB level at DC with the full bandwidth covered. The RF Rectifier uses the design principles of a cross-coupled rectifier and a 63% conversion efficiency is achieved with the proposed matching circuitry. The reference circuitry is designed with the Betamultiplier architecture and expanded slightly to improve the current consumption in the circuit. The reference current is set at 100 nA and reference voltage at 400 mV.

Keywords: RFID, Energy harvesting, EEG, ECG, Modular implant, LDO, Rectifier

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Langaton biosignaalien mittaus mahdollistaa yleisien lääketieteellisien signaalien mittauksien tehokkuuden kasvamista: Integroitu elektroninen piiri voidaan asentaa ihmisen kudokseen ja tämän sirun ulosantama tieto voidaan lukea langattomasti lukijalla, mikä useassa tapauksessa toimittaa myös energian sirulle. Tämä teknologia vaatii RFID teknologiaa, mikä on hyvin tunnettu ja tutkittu langattoman datan siirtämiseen kehitelty teknologia radiotaajuuksilla lukijan ja vastaanottimen välillä. Lukija voidaan suunnitella sekä passiiviseksi että aktiiviseksi, mutta modernin CMOS- teknologian tehonkulutus ominaisuuksien vuoksi RFID-lukijat ovat yleisesti passiivisia.
Passiivisessa RFID suunnittelussa lukija vastaanottaa tarvitsemansa energian vastaanottimelta yleisesti elektromagneettisen induktion avulla. 860 MHz UHF-kaistan suunnitelu ja toteutus käydään läpi tässä työssä ja suorityskyky on mitattu simulaatioilla. Itse järjestelmä oli alunperin suunniteltu langattomaan EEG-lukijaan (aivosähkökäyrä), minkä pystyisi asentamaan päänahan alle - mutta periaatteet pätevät mihin tahansa RF-kaistan järjestelmään.
Lopullinen järjestelmä toimii -6.8 dBm sisääntuloteholla ja käynnistysmisaika on hieman alle $40\mu s$ 700 mV ja 150 μA kuormaan. Linjaregulaatio saavuttaa -51 dB arvon alhaisilla taajuuksilla ja regulaatio on koko kaistan kattava. RF-tasasuuntaaja saavuttaa 63 % AC-DC huippu tehonmuutosarvon ehdotetulla impedanssien sovituspiirillä. Referenssipiiri on suunnitellu Betamultiplier-arkkitehtuurilla ja modifioitu pienentämään virrankulutusta. Referenssit ovat 100 nA ja 400 mV.

Avainsanat: RFID, Energiakeräys, EEG, ECG, Implantti, LDO, Tasasuuntaaja

Preface

First and foremost I want to thank my advisor D.Sc. Marko Kosunen and my supervisor Professor Jussi Ryynänen for the opportunity to work in Aalto University's Department of Electronics and Nanoengineering Circuit design unit. The abilities learnt during this project was more valuable than all the courses attended combined.

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Symbols and abbreviations

Symbols

α	Bandpass-filter damping factor
A_{DC}	Amplifier DC-gain
$A(s)$	Amplifier transfer function
β_R	LDO feedback resistor division constant
C_L	LDO output/load capacitance
C_{gd}	Gate-to-source capacitance
C_{sd}	Source-to-drain capacitance
C_p	Resonance crystal parallel capacitance
C_s	Resonance crystal series capacitance
f_p	Resonance crystal parallel oscillation frequency
f_s	Resonance crystal series oscillation frequency
g_m	Small-signal transconductance
g_{ds}/g_{sd}	Small-signal output conductance
g_{Rfb}	LDO feedback resistor total series conductance
$G(s)$	Feedforward transfer function
$H(s)$	Feedback transfer function
i	Imaginary unit
j	Imaginary unit
Ω	Ohm
ω	Angular frequency
ω_0	Dominant pole angular frequency
ω_{0a}	Opamp dominant pole angular frequency
$p_{0/1}$	Two-stage Opamp pole
Q	Bandpass-filter Quality-factor
R_{gd}	Small-signal output resistance
s	Laplace coefficient $j\omega$
$V_{amp\ out}$	Voltage at operational amplifier output
V_{ref}	LDO reference voltage

Abbreviations

AC	Alternating current
ADC	Analog-to-Digital Converter
CMOS	Complementary Metal-Oxide-Semiconductor
CMRR	Common-Mode Rejection Ratio
DC	Direct Current
ECG	Electrocardiography
EEG	Electroencephalography
FDSOI	Fully-depleted Silicon-on-Insulator
GBW	Gain-Bandwidth product
ICMR	Input Common-Mode Range
LDO	Low-Dropout Regulator
NFET/NMOS	N-type Field-Effect Transistor
Opamp	Operational amplifier
PCE	Power Conversion Efficiency
PGA	Programmable gain Amplifier
PSRR	Power Supply Rejection Ratio
PFET/PMOS	P-type Field-Effect Transistor
RF	Radio Frequency
RFID	Radio Frequency Identification
Si	Silicon
SiC	Silicon Carbide
SNDR	Signal-to-Noise plus distortion ratio
SNR	Signal-to-Noise Ratio
TADC	Time-based Analog-to-Digital Converter
UHF	Ultra high frequency
SVC	Self Threshold Voltage Cancellation
UGB	Unity Gain Bandwidth
VCO	Voltage Controlled Oscillator
VTC	Voltage to Time Converter

1 Introduction

Modular medical measurement platforms are an increasing opportunity for the monitoring of biosignals in patients. Installing a microsized integrated electrical circuit (IC) inside tissue creates vast possibilities for both medical professionals and patients: A medical professional can simply read biosignal data wirelessly and extract the information straight to database. For the patient, the implanted chip can be used to self-diagnose one's own medical condition by mapping the development of relevant human biosignals over time, such as Electroencephalography (EEG) or Electrocardiography (ECG). Wireless integrated circuits not only offer superior Signal-to-Noise Ratio (SNR) to older, non-invasive methods [1], but the convenience of not using bulky scalp electrodes for EEG measurements is a fascinating subject.

The techology used to wirelessly read, write and manipulate data quickly is called Radio-Frequency Identification (RFID). This technique is used all over the world from public transportation and card payments to more complex access monitoring systems found in many businesses and public facilities. RFID is a technique where electromagnetic field is used in radio frequencies to read and save data using RFID tags.

RFID tags come in two forms: active and passive. The difference between these two is that active tags require separate power supply (battery) inside the receiver. The passive RFID tags are (often) based on inductive power transform in which an antenna is integrated on the chip. This severely eases the burden of any possible medical applications in which these chips might be used, since active tags would require recharging in certain time intervals. Batteries for example often contain harmful materials that could dissolve in living tissue causing harmful side effects in the patient [2]. The induction based power transform only uses electromagnetic fields that with small intensities are harmless to living tissue. The power available for the tag antenna is then transformed into a DC voltage that supplies the rest of the chip components. In this work the design principles of the aformentioned AC-to-DC power transformation is studied in the Ultra High Frequency band (UHF).

In section 2 the required theory for this work is presented. The EEG RFID system presented in [2] is briefly discussed first, which is followed by the working principle of the AC-to-DC power conversion. The power harvesting system consists of 1) a rectifier, which design is presented in section 3 and 2) a regulator, presented respectively in section 4. In section 5 the parts are implemented based both on theory and their layouts are carried.

The main design goals were to maximize the efficiency of the system while demanding full bandwidth regulation. The impedance matching is performed to an ideal power source (50 Ω single-ended, 100Ω differential) and the final design load is an oscillating current source oscillating at 1 MHz frequency, drawing 150μA of DC current.

2 Background

The inspiration for this thesis arose due to work performed for a power section for an RFID EEG-reader. EEG is the measurement of the potential fluctuations in the brain. EEG has many uses in the field of medicine such as identifying epilepsy [3], hand motor functions [4] [5], brain death [6] and sleep disorders [7]. EEG-signal analysis is heavily depended on signal processing due to the inherently noisy nature of the signal and new algorithms are constantly being created to increase the SNR. In an RFID EEG-reader, the power system must provide stable and noise-free supply for the sensitive analog parts of the system which mainly consist of the Analog-to-Digital Converter (ADC). The most sensitive digital processing parts can be initiated inside the chip but the more complex computations can be outsourced after the EEG signal has been converted and sent back to the receiver.

2.1 EEG Measurement System

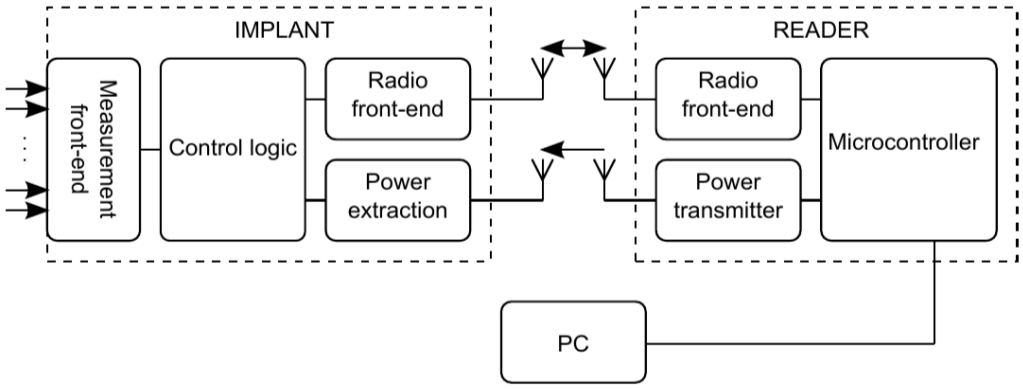


Figure 1: EEG System Block Diagram [2]

The complete system is depicted in Fig. 1 as a block diagram. The system comprises of measurement front-end (ADC and filtering), control logic, radio front-end and energy harvesting units on which the latter this thesis is based on. EEG signals are detectable generally in the very low-frequencies of around 1-100 Hz, however due to the inherent flicker noise (1/f noise) in electronic systems the extreme low frequencies should be removed by either filtering or noise shaping techniques such as chopper amplifiers [8]. Other low-frequency artefacts such as small movement and breathing are also taken into account in the system [2].

The sensing electrodes are connected directly to a sensitive instrumentation amplifier with both very high input impedance and high common-mode rejection ratio (CMRR) to accommodate the skin impedance and natural noise generation from the subject [9, 2]. Four electrodes are used and each electrode drives the instrumentation amplifier that in turn drives a bandpass filter which goes into a

multiplexer where the desired input is chosen by control logic. Multiplexer output drives a programmable gain amplifier (PGA) to further boost the signal before the ADC. Conversion circuit is based on time-domain conversion that switches the direction of integration in the Voltage Controlled Oscillator (VCO) when a bit is detected. Another possible implementation of TADC (Time-based Analog-to-Digital Converter) is to switch the VCO with an VTC (Voltage-to-Time Converter) which will provide a better linearity but worse SNDR (Signal-to-noise plus distortion ratio) [10].

Initially the communication and power extraction were designed to operate on two different channels: The 6.75 MHz ISM band and the 865 MHz UHF band [2]. This work focuses only on the UHF band extraction and the simulations are performed with 860 MHz input frequency (due to some initial communication discrepancies) - however the tuning is accessible easily since no on-chip matching is performed.

In the initial design, Class-E power amplifier is used to drive the transmitter output antenna at the ISM band. Class-E is a resonant power amplifier design in which two separate resonant frequencies are created by switching the power amplifier on and off with a gate driver [11] [12] [2]. The gate driver digital signal is then converted into a constant current sinusoidal signal in the output resonator circuit.

The opening section discussed the operation principle of the EEG measurement system depicted in Fig. 1 and the subsequent sections will examine the necessary functions to provide the power management of the system through RF energy harvesting, of which the central piece is the Low-Dropout Regulator (LDO).

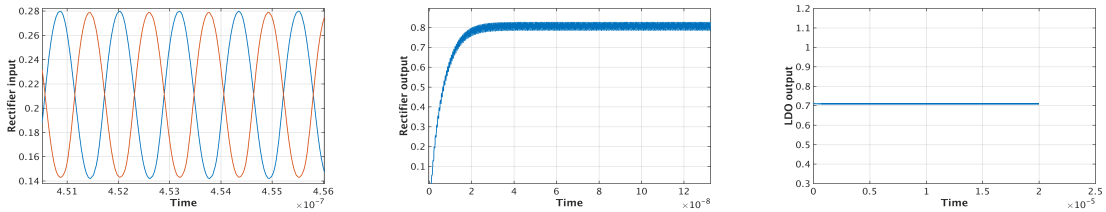
2.2 RF Energy Harvesting

RF energy harvesting -section provides the background information to understand the fundamental principles of the separate systems required for an RFID power system. In section 3, section 4 and section 5 these concepts are examined, the theory presented and finally implemented. The system is implemented with a 28 nm FDSOI-process and the required components for the system described are:

- Rectifier
- Low-Dropout Regulator (LDO), which consists of
  - An Operational Amplifier (opamp)
  - A Voltage Reference
  - A Current Reference

The purpose of the rectifier is to transform the radio frequency signal energy, received by the antenna, to a reasonable DC-level for the LDO to operate correctly. LDO's function is to provide a stable DC-voltage for the chip all the while suppressing any unwanted variations at the output.

In this work, the current- and voltage references are taken from the same Beta-multiplier -based circuit as the low power consumption is one of the main objectives



(a) *Differential RF in* (b) *Rectified output* (c) *LDO output*

Figure 2: *Functional illustration of the system*

of the design. The output of the reference is not buffered since the initial design did not require strict isolation to physical surroundings and the reference nodes have a fairly high capacitance to AC-ground (large transistors and added capacitors).

The operational amplifier is designed to balance the bandwidth and gain to achieve a wide regulation bandwidth. Operational amplifier designs studied in this work are the single-stage differential amplifier and the two-stage Miller-compensated operational amplifier. The chosen operational amplifier implementation for this work is the single-stage differential amplifier which is designed to balance the bandwidth and gain to achieve a wide regulation bandwidth.

Operational amplifier design gets harder as the supply voltages are dragged down along the linewidth reduction. Operational amplifiers are used everywhere such as ADC's, DAC's, comparators and integrators. LDO design often requires high gain, high bandwidth cascode amplifiers, which have the highest gain and can effectively reduce the Miller effect [13]. Cascode amplifiers usually require a large number of transistors over the available supply and with small supplies that option is not viable.

2.3 Goals

In this work, a differential RF-Rectifier and an LDO is designed to provide 0.7 Volts of supply voltage for an analog- and digital circuitry drawing around 150 μA of DC current. This would make the total load power consumption 105 μW. There will be oscillating components in the load at 1 MHz. The load can then be modelled as an oscillating current source for the LDO simulations.

Due to the varying input voltage and load current, the line and load regulation are important parameters and are discussed in detail in section 4. The line regulation refers to LDO's ability to suppress variations at the input and conversely load regulation refers to the ability of output variation suppression. Good regulation performance requires high opamp gain and bandwidth in addition with very high load capacitance.

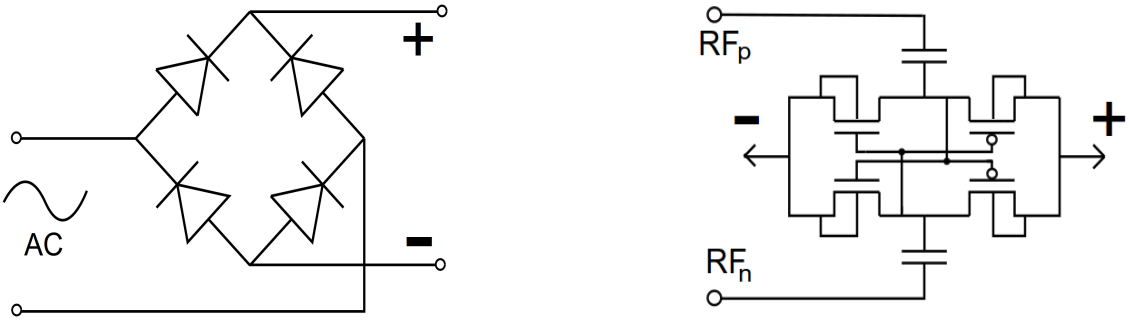
Temperature variance compensation is not taken into account. Such compensation is required mostly in the reference circuitry and are discussed in [14, 15, 16, 17]. The RF frequency for this work is 860 MHz and at these frequencies the input impedance of the rectifier can be compensated with technique presented in section 3.

3 RF Rectifier

RF rectifier is an electronic component which sole purpose is to direct the energy of the input RF-signal to a desired DC-level. The *diode* is the main component used to construct a rectifier. In Fig. 3a four diodes are arranged in such a method that the positive phase of the AC-signal is directed to the + -terminal and the negative phase to the − -terminal. The output of this configuration is the half-wave rectified signal as shown in Fig. 2b.

RF Rectifiers have been studied extensively in [18] [19] [20] [21] [22]. One of the best known rectifier structure is the *cross-coupled* rectifier shown in Fig. 3b. This structure offers a low-on resistance and excellent efficiency for low input power. This structure is also known as *Self V_{th} Cancellation (SVC) Rectifier*. In SVC Rectifier the NMOS- and PMOS transistors are arranged in pairs: The positive (upper) phase PFET will conduct when the negative input is low, since the gates are *cross-coupled*. This differs from earlier RF Rectifier designs, where FET gates are connected to either common (PMOS) or output (NMOS). The operation of the SVC is as follows: when the positive input goes low, the NMOS in the same side will conduct because the negative input is high. The main improvement of this structure is the threshold voltage V_{th} cancellation which is achieved by connecting 1) the PMOS bulk to the higher potential +-terminal and 2) the gate to the lowest/highest potential possible according to the phase of the input signal.

The downside of this architecture is the high required input voltage amplitude, which must be generally higher than the threshold voltage V_{th}. For more lower input power applications the standard FET's should be replaced with HTFET's (Heterojuction Tunnel Field Effect Transistors) reported in [22]. These transistors offer operation at low input power ranges, reaching as low as -33 dBm input power sensitivity.



(a) *A Diode Bridge* (b) *CMOS Rectifier*

Figure 3: *A diode bridge translates to a CMOS RF Rectifier*

3.1 Rectifier parameters

RF rectifier's most important performance parameters are:
1. AC-to-DC Power Conversion Efficiency PCE

2. Input Impedance
3. Transistor Sizing.

Their definitions and behaviour are reviewed in subsequent subsections. The performance parameters are obtained with transient simulations, using a power source in input and a resistor and a parallel capacitor in the load. Voltage source simulations can be performed in order to gain more information about the PCE/input voltage ratio [23].

3.1.1 PCE

The power conversion efficiency is the amount of DC power available for the load with respect to input power. In [19] the PCE is defined as:

$$PCE = \frac{P_{out}}{P_{in}} = \frac{P_{out}}{P_{out} + P_{loss}} = \frac{P_{out}}{P_{out} + N \cdot P_{diode}}, \tag{1}$$

where N is the number of diode stage and P_{diode} is the power loss in an individual diode. The ON-Resistance of the Diode is the most contributing factor to this power loss. The diode loss can be minimized by: 1) a wider transistor, 2) optimal gate biasing and or 3) optimal bulk biasing. The cross-coupled connection satisfies optimal gate biasing and transistor width. However, it is possible to create even more efficient rectifier structures based on the cross-coupled rectifier such as the forward-biasing technique demonstrated in [23] and shown in Fig. 4. In this technique the bulk connections are inverted so that in the single-stage rectifier the PMOS bulk connection is at the common node and the NMOS bulk connection at output node and satisfies the forward biasing equation $V_{sb} < 0$. The forward biasing technique is recommended for low input power applications since it decreases low input voltage threshold. For less demanding load conditions, if the input voltage threshold is not a main concern, the standard bulk biasing would offer superior PCE performance with higher input power levels [23].

Due to high threshold voltage of standard CMOS transistors, rectifiers have been generally implemented with Schottky diodes. Schottky diodes have a much lower threshold voltage creating a superior input sensitivity - thus PCE. It wasn't until the cross-coupled, V_{th} cancelling scheme presented in [19] that allows more cost-efficient design for RF rectifiers (generally Schottky diodes are not compatible with standard CMOS manufacturing processes).

3.1.2 Input Impedance

At radio frequencies, the input matching must be carried out to achieve a desired power conversion efficiency. The most fundamental property of impedance matching is the cancellation of the imaginary part and matching the real part of the input impedance as in (2).

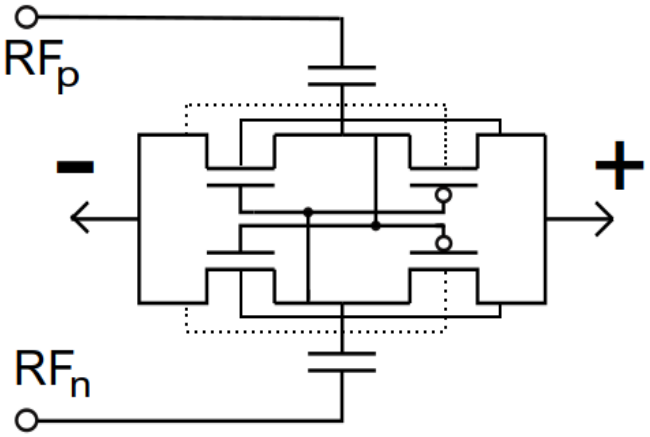


Figure 4: Forward biased RF rectifier

$$Z_s = Z_{in}^* \tag{2}$$

The fundamental theory for impedance matching is well established.

Input impedance behaviour of the rectifier is not linear with respect to input power [24] but the nonlinear effects are more present in applications requiring very high RF input power [25].

For this work, a simple LC-technique can be taken into use to match the ideal power source and the rectifier to provide reasonable power conversion results. The impedance of the antenna is assumed to be 100Ω since the system is fully differential.

To estimate the input impedance, it is suggested to take a look at the single ended model at Fig. 21a and 21b. Without the proposed matching circuit, the power source sees only the input capacitor which will add negative phase for the input voltage (Fig. 21a). The value of this phase shift is the value of the impedance of the input capacitor C_i:

$$Z_{C_i} = \frac{1}{j\omega C_i}, \tag{3}$$

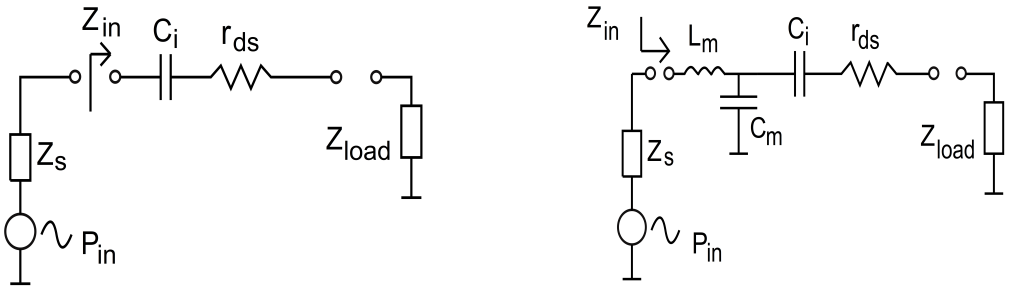
where j is the imaginary unit, ω the angular frequency 2πf and C_i the value of the capacitor. To cancel this impedance, an inductive circuit element should be added. The input capacitors should be rather large to maximize efficiency and to avoid unnecessary large inductor values, a parallel capacitor is also introduced so that the imaginary part of input impedance seen by the power source, is the sum of the inductor and parallel capacitors (Fig. 21b):

$$\Im(Z_{in}) = j\omega L_m + \frac{1}{j\omega C_m} \,||\, \frac{1}{j\omega C_i} = j\omega L_m + \frac{1}{j\omega(C_m + C_i)} \tag{4}$$

Let the leftmost side of (4) be zero, so the inductor value will be:

$$L_m = \frac{1}{\omega^2(C_m + C_i)} \tag{5}$$

For this work, the other parameters (channel resistance and load impedance) are not taken into account as it is most important to avoid the reflections at the input interface, than after available power has entered the rectifier. The results for the impedance matching scheme can be seen in section 5.



(a) *Input impedance seen without matching* (b) *Proposed matching circuit*

Figure 5: *The single-ended input impedances of the rectifier*

The Q-factor of a matching circuit describes how underdamped the resonant circuit is (the width of the resonance band) and a high Q-factor means higher rate of energy transfer in the circuit. Generally it is recommended to avoid using microstrip IC-inductors as impedance matching components due to the low Q-factor of microchip inductors. For example capacitors can achieve a Q-factor over 1000 and a resonance crystal Q-factor can to go to 80000 at 13-14 MHz [26]. Compare this to standard on-chip inductors, where the Q-factors are generally only 200 [26] - even with advanced manufacturing techniques. All the simulations in this work are performed with ideal inductors, so the PCE will be noticeably lower with the actual inductor, whether a typical IC-inductor or an alternative is chosen for matching component.

Also to bear in mind is that a high Q-factor posesses a problem for biosignal measurement: High data rate requires high bandwidth and high power transfer lower frequencies, as the tissue absorption at lower frequencies is lower than UHF band absorption [2] [27] [28].

For UHF band applications, it is recommended to take a look at possible applications of MEMS-based monolithic crystals presented in [29], where 300-400 MHz fQ (frequency-Q -factor product) of $4 \cdot 10^{12}$ was achieved.

Crystal has an equivalent circuit of a parallel C - to LCR -circuit creating two resonant frequencies f_p and f_s and their values are presented in (6). The single parallel capacitor C_p is the value of a shunt capacitor. The motional values of the crystal are then the series components L, R and C_s.

$$f_s = \frac{1}{2\pi\sqrt{LC_s}} \tag{6a}$$

$$f_p = \frac{1}{2\pi\sqrt{L\frac{C_sC_p}{C_s+C_p}}} \tag{6b}$$

3.1.3 Transistor sizing

The size of the transistor affects both the 1) ON-Resistance of the diode and 2) parasitic capacitances. Sizing up the width of the transistors diminished the resistive losses, however too large transistors can have dominating parasitic capacitances at radio frequencies. By adjusting the sizing, the designer can shift the PCE-peak to the desired output power value defined by the load. More of this is in section 5.

4 Low-Dropout Regulator

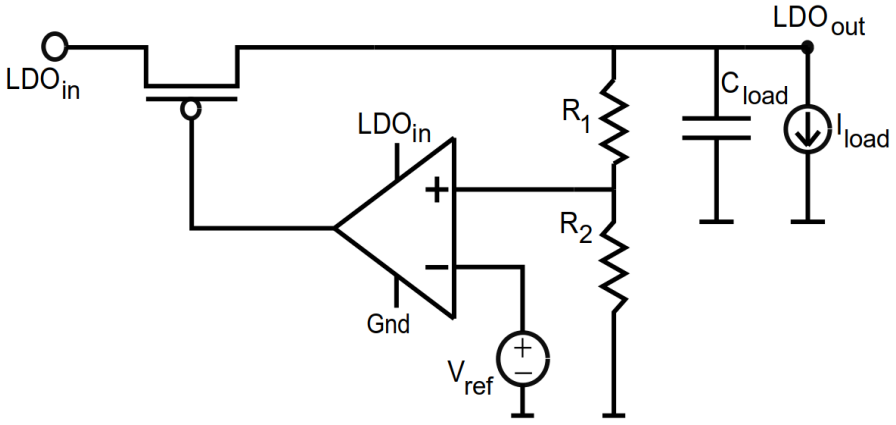


Figure 6: PFET Low-Dropout Regulator

Fig. 6 depicts the standard Low-Dropout Regulator (LDO) system schematic. The input PFET's gate is controlled by the operational amplifier, which in turn is configured in a negative feedback loop trough the resistor-based voltage divider network (negative due to the operation of the PMOS transistor). The feedback loop ensures that the output voltage remains at a desired level all the while suppressing external AC signals entering the circuit. The load current I_{load} represents the desired current consumption of the analog and digital processing parts of the circuit. The load capacitance C_{load} is a very large capacitor that keeps the LDO loop stable at high frequencies.

The operation principle is given in Fig. 7, where the output voltage is given as a function of input voltage. A low dropout voltage is one of the most desirable functions of an LDO as the dropout voltage mainly determines the power loss in the circuitry due to high currents drawn from the rectifier. Power consumption optimization can be achieved by designing the error amplifier and reference circuitry with low supply voltages, and using the widest possible pass-transistor achievable.

What makes very low-dropout through the pass-FET possible, is the ability to use small gatelength power-FET in modern CMOS processes, as the length of the channel is directly proportional to the channel resistance. For reference, the high power-FET used in this work has a gatelength of 150nm, which is still small compared to older processing techniques not even 5 years ago. LDO studies have been conducted in [13, 30, 31, 17, 32]

4.1 Operation principle and line regulation

The most simplified model of the DC operation is based on the ideal operational amplifier analysis: In negative feedback, the operational amplifier drives the differential input voltage to zero. Considering the voltage-divider circuit at the output, the plus-terminal of the error amplifier will be as in (7).

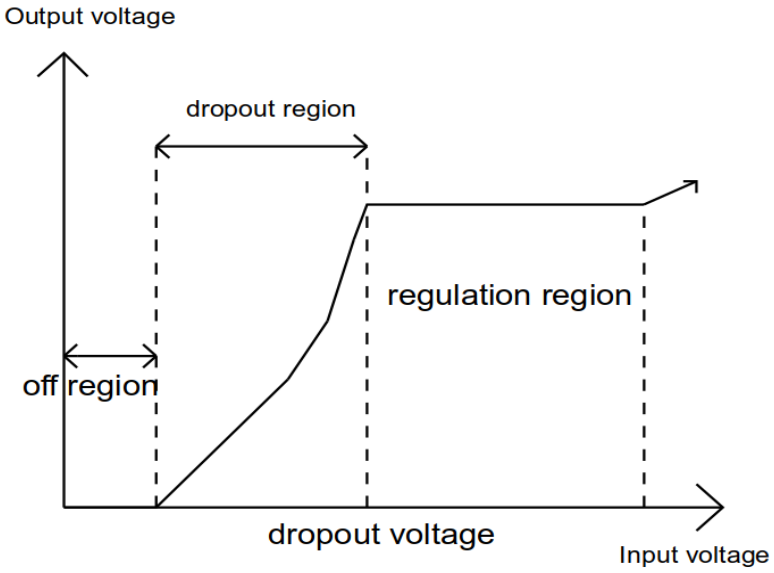


Figure 7: Operation regions of an LDO

$$V_+ = V_{out}\left(\frac{R_2}{R_1 + R_2}\right) \tag{7}$$

And if $V_+ = V_- = V_{ref}$, then the output voltage will set to:

$$V_{out} = V_{ref}\left(1 + \frac{R_1}{R_2}\right) \tag{8}$$

With limited amount of amplifier gain available, there exists an input DC-level range for each individual LDO. If the input voltage exceeds this threshold, the amplifier can not supply enough gain for the control loop, the drain-source conductance of the pass-transistor will not change, leading to lesser rate-of-change in source-to-drain voltage and the LDO will go out of regulation region. The relationship between the gain of the amplifier and line regulation can be derived with the circuit analysis performed on open load as in Fig. 8.

In the open-circuit analysis, the drain current of the PMOS will go through the

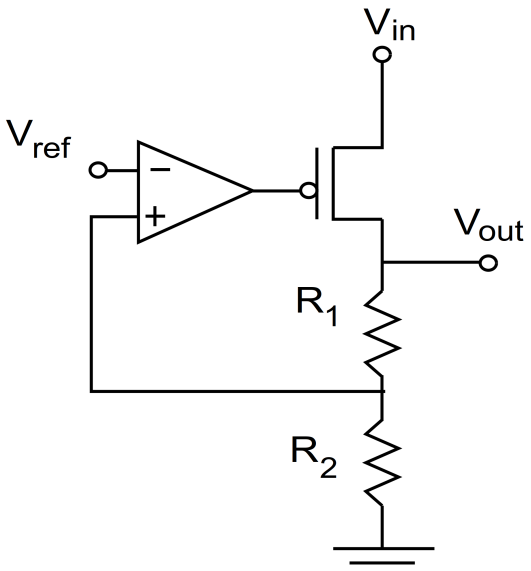


Figure 8: LDO open-load analysis

feedback resistors so following equations can be written:

$$V_{out} = Id(R_1 + R_2) \tag{9a}$$
$$V_+ = V_{out}\frac{R_2}{R_2 + R_1} \tag{9b}$$
$$V_g = A(V_+ - V_{ref}) \tag{9c}$$
$$I_d = g_m V_{sg} \tag{9d}$$
$$V_s = V_{in}, \tag{9e}$$

where A is the open-loop gain of the operational amplifier and g_m the transconductance small-signal parameter of the PFET. At this point, the effect of parasitic capacitances are not taken into account.

If (9b) is substituted into (9c) and (9d) into (9a), V_{out} can be expressed as:

$$V_{out} = g_m(V_{in} - A(V_{out}\frac{R2}{R1 + R2} - V_{ref}))(R_1 + R_2) \tag{10}$$

Solving (10) as V_{out}, we get:

$$V_{out} = \frac{g_m A(R_1 + R_2)}{g_m R_2 A}V_{ref} + \frac{g_m(R_1 + R_2)}{1 + g_m R_2 A}V_{in} \tag{11}$$

Assuming that $g_m R_2 A >> 1$:

$$V_{out} = (1 + \frac{R_1}{R_2})V_{ref} + \frac{(1 + \frac{R_1}{R_2})}{A}V_{in} \tag{12}$$

Eq. (12) has two parts: The DC-reference voltage component and the AC line regulation (with respect to V_{in}). Optimal operation is obtained when AC line regulation is minimized.

If the operational amplifier behaviour is modelled as a single-pole low-pass filter with gain A_{DC}:

$$A = A(s) = \frac{A_{DC}}{1 + \frac{s}{\omega_{0a}}}, \tag{13}$$

the AC line regulation part of (12) can be expressed as:

$$\text{AC line regulation} = \frac{(1 + \frac{R_1}{R_2})(1 + \frac{s}{\omega_{0a}})}{A_{DC}} \tag{14}$$

In (14) a zero is created at the amplifier's pole ω_{0a}, which means that without any compensation, the system would introduce gain at high frequencies. The amplifier's pole is created by driving the parasitic capacitances of a very large LDO transistor, which can have gate capacitances in 10^2 fF magnitude range.

To improve line regulation, it is seen that high open-loop gain and high bandwidth from the amplifier is required along with a pole that must be introduced to the system. $\frac{R_1}{R_2}$ -ratio should also be kept at minimum but this ratio is defined by the required output voltage and reference voltage ratio as in (8).

4.2 AC Line Regulation with parasitics and load capacitance

The theory presented earlier should be expanded into a full small-signal model with added capacitors. The reference voltage is assumed to be an ideal DC source so it is grounded. The used model is given in Fig. 9. The load is modelled as a conductance and for the following calculations the load is assumed to be infinite. The added load capacitor will be very large compared to the parasitics.

When AC resistance of the load is considered infinite ($g_L = 0$), the current equations for the system in Fig. 9 can be written as:

$$I_{in} = I_d = g_m V_{sg} + (g_{sd} + sC_{sd})(V_{in} - V_{out}) \tag{15a}$$

$$I_{out} = V_{out}(sC_L + \frac{1}{R_1 + R_2}) \tag{15b}$$

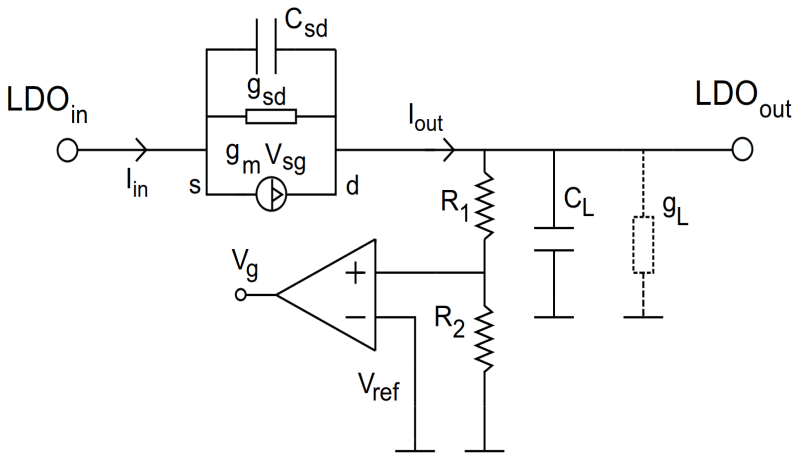


Figure 9: LDO s-domain model

Substituting V_{sg} as was performed in (9), we get:

$$I_{in} = g_m V_{in} - g_m A(s)\beta_R V_{out} + g_{sd}(V_{in} - V_{out}) + sC_{sd}(V_{in} - V_{out}) \tag{16a}$$
$$I_{out} = V_{out} sC_L + V_{out} g_{Rfb}, \tag{16b}$$

where g_{Rfb} is the total conductance of the feedback network. With these equations, the transfer function can be solved as:

$$\frac{V_{out}}{V_{in}} = \frac{g_m + g_{sd} + sC_{sd}}{g_m A(s)\beta_R + g_{sd} + g_{Rfb} + s(C_L + C_{sd})}, \tag{17}$$

where β_R is the voltage division constant between R_2 and R_1.

By approximating the transfer function of the operational amplifier to be the following:

$$A = A(s) = \frac{A_{DC}}{1 + \frac{s}{\omega_{0a}}},$$

then (17) will assume the following form:

$$\frac{V_{out}}{V_{in}} = \frac{(g_m + g_{sd} + sC_{sd})(1 + \frac{s}{\omega_0})}{A_{DC} g_m \beta_R + s(C_L + C_{sd})(1 + \frac{s}{\omega_0}) + (g_{sd} + g_{Rfb})(1 + \frac{s}{\omega_0})} \tag{18}$$

Assuming the conditions that $C_{sd} \approx 0$ and $g_{Rfb} << g_{sd}$, (18) can be written as:

$$\frac{V_{out}}{V_{in}} = \frac{g_m(1+\frac{s}{\omega_{0A}})}{s^2\frac{C_L}{\omega_{0A}} + s(C_L + \frac{gsd}{\omega_{0A}}) + (g_{sd} + A_{DC}g_m\beta_R)} \tag{19}$$

To simplify the transfer function, divide by C_L/ω_0 and set $g_m A_{DC}\beta_R >> g_{sd}$:

$$\frac{V_{out}}{V_{in}} = \frac{\frac{g_m\omega_{0A}}{C_L}(1+\frac{s}{\omega_{0A}})}{s^2 + s(\omega_{0A} + \frac{g_{sd}}{C_L}) + \frac{g_m A_{DC}\beta_R\omega_{0A}}{C_L}} \tag{20}$$

Eq. (20) resembles the transfer function of a bandpass-filter:

$$H(s) = \frac{H_0\frac{\omega_0}{Q}s}{s^2 + s\frac{\omega_0}{Q} + \omega_0^2} = \frac{H_0\frac{\omega_0}{Q}s}{(s+\frac{\omega_0}{2Q})^2 + \omega_0^2 - (\frac{\omega_0}{2Q})^2}, \tag{21}$$

where ω_0 in (21) is the oscillation frequency, or the center frequency of the filter. Term $\frac{\omega_0}{Q}$ describes the width of the filter band and H_0 the gain of the filter.

The transfer function (20) with approximated parameter values is plotted with Matlab and presented in Fig. 10. The calculated bandwidth and oscillation frequency are correctly corresponding with the Matlab values.

If it is assumed that the denominator of the rightmost side of (21) will satisfy the condition:

$$\frac{\omega_0}{2Q}^2 << \omega_0^2,$$

which in this case is two order of magnitudes, the denominator will be further simplified to:

$$D(s) = (s + \frac{\omega_0}{2Q})^2 + \omega_0^2 \tag{22}$$

The term $(s+\frac{\omega_0}{2Q})^2$ in (22) can be written as $(s+\alpha)^2$, where α denotes the *damping factor* of the system. Therefore, when excited with an input step response, the damping factor of the system is approximately:

$$\alpha = \frac{\omega_{0a} + \frac{gsd}{C_L}}{2} \tag{23}$$

So far, this section has derived a bandpass-filter approximation for the LDO transfer function. The list of conclusions from the equations are presented below:

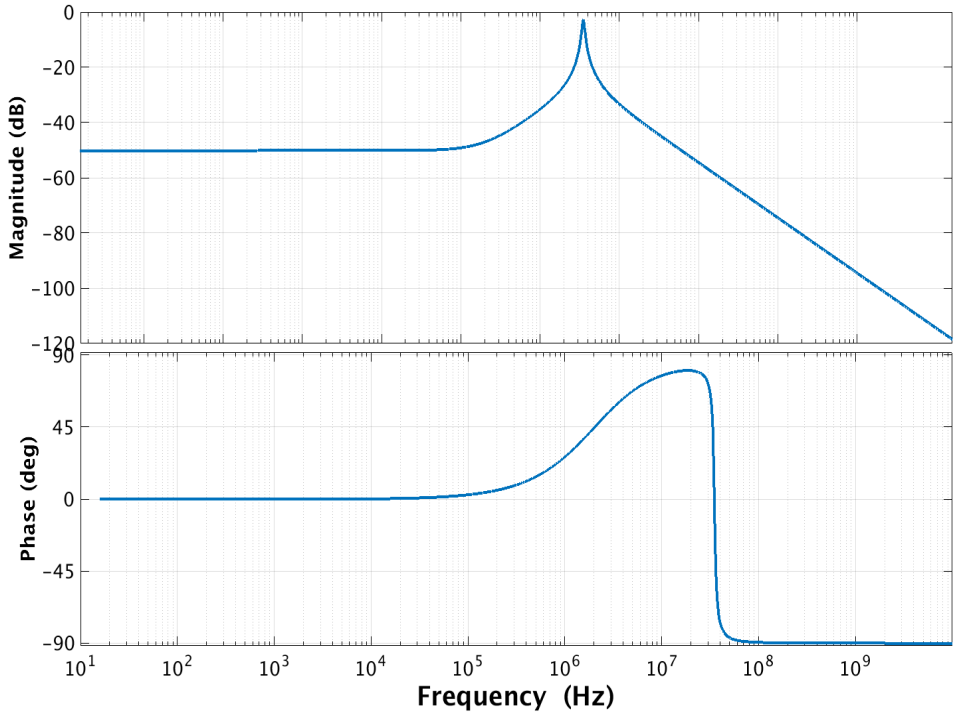


Figure 10: *Frequency response of (20) with approximate values*

- The (first) zero of the system is defined by the opamp pole ω_{0a}
- The oscillation frequency is described by the term

$$\omega_0 = \sqrt{A_{DC}\omega_{0a}g_m\beta_R/C_L}$$

- The width of the band is then given by the term

$$\Delta\omega = \frac{\omega_0}{Q},$$

where

$$Q = \frac{\omega_0}{\omega_{0a} + g_{sd}/C_L}.$$

Therefore

$$\Delta\omega = \omega_{0a} + \frac{g_{sd}}{C_L}$$

- By setting $s \to 0$ to inspect DC gain of the system, the transfer function reduces to

$$H(s \to 0) = \frac{1}{A_{DC}\beta_r},$$

which is the same as (14) in low frequencies.

- At oscillation frequency, where $s = \omega_0$, the LDO will have a transfer function of the form of:

$$|H(s = j\omega_0)| = \frac{g_m/C_L}{\omega_{0a} + g_{sd}/C_L},$$

and if you consider that the opamp has very low frequency dominant pole, we obtain:

$$|H(s = j\omega_0, \text{low } \omega_{0a})| = \frac{g_m}{g_{sd}}.$$

This means it is recommended to minimize the g_m/g_{sd} -ratio of the pass transistor as it will behave like a common-gate amplifier in frequencies above feedback loop UGB. With very high operational amplifier bandwidth, this problem can be remedied. Now, if the MOSFET is considered to be in saturation, the term g_m/g_{ds} can be minimized by observing:

$$\frac{g_m}{g_{ds}} = \frac{K\frac{W}{L}(V_{SG} - |V_{th}|)}{K\frac{W}{2L}(V_{SG} - |V_{th}|)^2\lambda_p} = \frac{2}{(V_{SG} - |V_{th}|)\lambda_p},$$

which indicates that a high source-to-gate (V_{SG}) voltage in the DC operation point is desired.

Fig. 11 represents when the pole of the opamp ω_{0a} is shifted to lower frequencies in the transfer function (in the case of the circuit, the gate capacitance is increased).

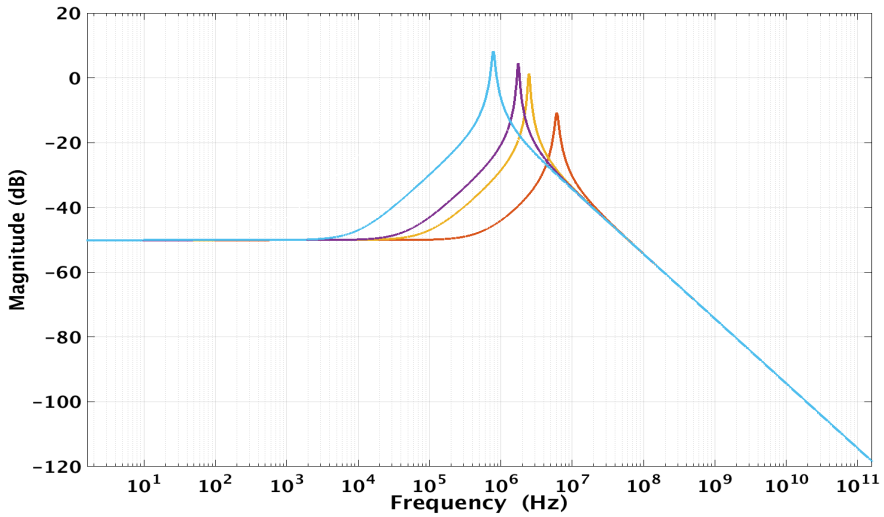


Figure 11: Decreasing opamp pole results in higher resonator gain and lower resonance frequency due to the zero of (14)

4.2.1 Two-Stage Opamp

The two-stage Miller-compensated operational amplifier has a transfer function of the form of [33]:

$$H(s) = \frac{A_{DC}(1 + \frac{s}{z0})}{(1 + \frac{s}{p0})(1 + \frac{s}{p1})} \tag{24}$$

If (24) is inserted into (17), the transfer function will obtain the following form:

$$\frac{V_{out}}{V_{in}} = \frac{g_m(1+\frac{s}{p_0})(1+\frac{s}{p_1})}{s^3\frac{C_L}{p_0p_1}+s^2(C_L(\frac{1}{p_0}+\frac{1}{p_1})+\frac{g_{sd}}{p_0p_1})+s(C_L+g_{sd}(\frac{1}{p_0}+\frac{1}{p_1})+\frac{g_m\beta_R A_{DC}}{z_0})+g_{sd}+g_m A_{DC}\beta_R} \tag{25}$$

In (25) the terms $p_{0,1}$ and z_0 refer to the two poles and zero of the two-stage opamp. Fig. 12 depicts the frequency response of (25) with and without the s^3 term.

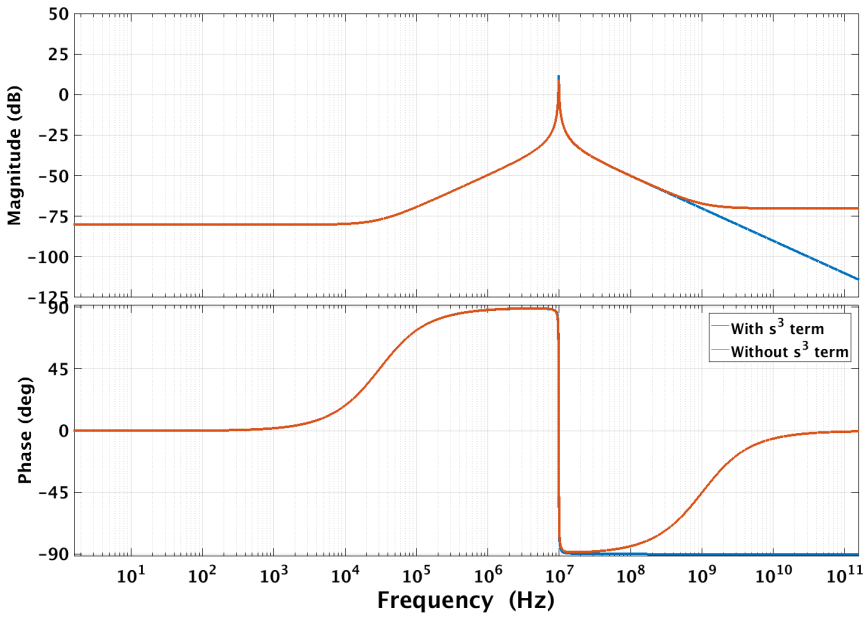


Figure 12: LDO transfer function with a two-stage amplifier. A higher Q-value resonant peak is created and > 0 dB line regulation is possible

Third order term can be neglected for analysis purposes, since the magnitude of C_L is in pF and the pole product p_0p_1 is very large and this is verified in Fig 12. This does not affect the bandpass resonance frequency.

If the s^2 term in (25) is divided to obtain a bandpass form denominator, the function will assume the form as in (26). In this form, the transfer function will still reduce to the first-order opamp form if p_1 and z_0 are very large.

$$\frac{V_{out}}{V_{in}} = \frac{g_m(1+\frac{s}{p_0})(1+\frac{s}{p_1}) \cdot \frac{1}{C_L(\frac{1}{p_0}+\frac{1}{p_1})+\frac{g_{sd}}{p_0 p_1}}}{s^2 + s(\frac{C_L+g_{sd}(\frac{1}{p_0}+\frac{1}{p_1})+\frac{g_m\beta_R A_{DC})}{z_0}}{C_L(\frac{1}{p_0}+\frac{1}{p_1})+\frac{g_{sd}}{p_0 p_1}}) + \frac{g_m\beta_R A_{DC}}{C_L(\frac{1}{p_0}+\frac{1}{p_1})+\frac{g_{sd}}{p_0 p_1}}} \tag{26}$$

Which can yet be further reduced into:

$$\frac{V_{out}}{V_{in}} = \frac{\frac{g_m p_0 p_1}{C_L(p_0+p_1)+g_{sd}}(1+\frac{s}{p_0})(1+\frac{s}{p_1})}{s^2 + s(\frac{C_L p_0 p_1 + g_{sd}(p_0+p_1)}{C_L(p_0+p_1)+g_{sd}}) + \frac{A_{DC} g_m \beta_R p_0 p_1}{C_L(p_0+p_1)+g_{sd}}} \tag{27}$$

Observing that the common denominator term $C_L(p0+p1)+g_{sd}$ can be reduced into $C_L(p0+p1)$ since $g_{sd} << CL(p0+p1)$. This gives a convenient transfer function that equals that with single-stage opamp transfer function if $p_1 >> p_0$.

$$\frac{V_{out}}{V_{in}} = \frac{\frac{g_m}{C_L} p_0||p_1(1+\frac{s}{p_0})(1+\frac{s}{p1})}{s^2 + s(p_0||p_1 + \frac{gsd}{C_L}) + \frac{A_{DC} g_m \beta_R}{C_L} p_0||p_1}, \tag{28}$$

where

$$p_0||p_1 = \frac{p_0 p_1}{p_0 + p_1}$$

From here it is possible to identify the familiar parameters ω_0, $\Delta\omega$ and peak gain at $s = j\omega_0$ as with the single stage model.

$$|H(s=j\omega_0)| = \frac{g_m/C_L}{p_0||p_1 + g_{sd}/C_L}$$
$$\omega_0 = \sqrt{\frac{A_{DC} g_m \beta_R}{C_L} p_0||p_1}$$
$$\Delta\omega = \omega_0/Q = p_0||p_1 + \frac{g_{sd}}{C_L}$$

4.3 AC Load regulation

The concept of load regulation arises from the fact that changes in the load current can happen, either unintentionally or by design. Small signal load regulation is the output impedance of the LDO and can be measured by current equations and shorting the input to ground. The configuration is shown in Fig. 13

The current equation is:

$$I_{fb} = I_{out} - V_{out} s C_L - g_m V_g,$$

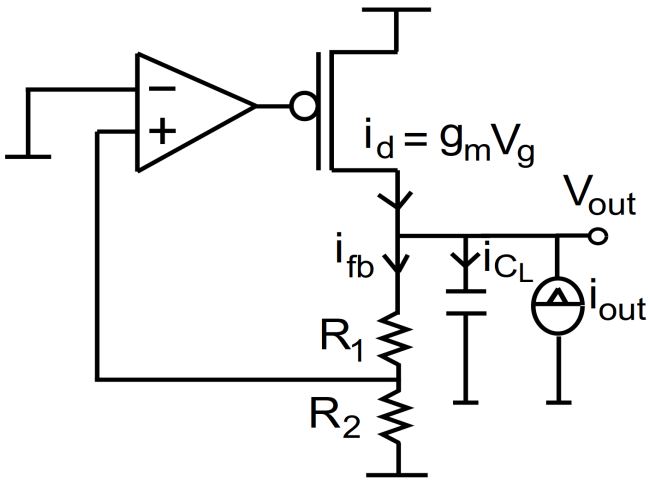


Figure 13: Output impedance/Load regulation measurement configuration

where $V_g = A(s)\beta_R V_{out}$
Solving these current equations with respect to V_{out}/i_{out} will be:

$$Z_{out} = \frac{1}{sC_L + g_m A(s)\beta_R + \frac{1}{Rfb}} \tag{30}$$

The general curve for output impedance is a bandpass filter as is line regulation. Low output impedance is desired as it describes how sensitive the output voltage is with respect to changes in load current. Output impedance can therefore be improved with 1) high opamp gain, 2) high pass PMOS transconductance and 3) stable reference voltage.

Load regulation is dependent on the size of the load resistor/load current: Regulation ability drops with higher load current. In this work, the measured load regulation is measured with the $150\mu A$ DC value.

4.4 Negative feedback stability

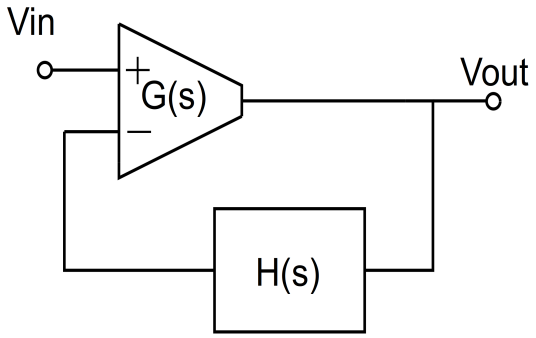
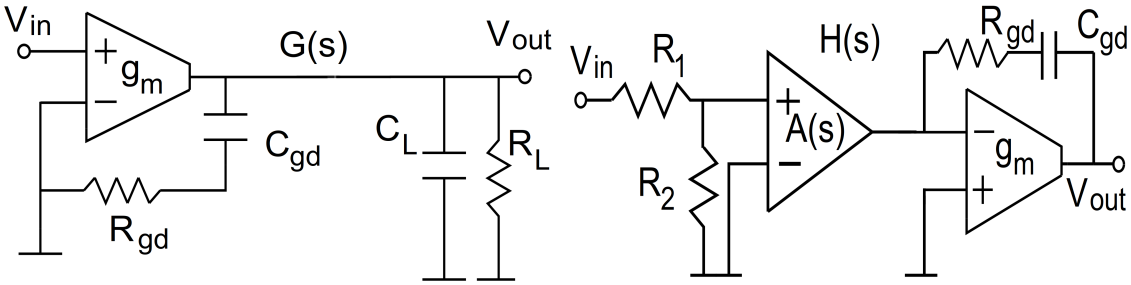


Figure 14: Negative feedback

For stability analysis, the negative feedback *feedforward* and *-back* paths should be identified. In Fig. 14, the common feedback schematic model is presented. In this section, paths are analyzed and the root-locus of the system is estimated (subsection 4.4.1).

The feedforward path consists of the transconductance input stage and the load as in Fig. 15a. In the feedforward path, the feedback resistors R_1 and R_2 are very large compared to the load so they are left open.

The feedback loop consists of the resistor divider network and the operational amplifier. It is also required to add the zero/pole pair that is created due to the very large PMOS transistor's gate-to-drain capacitance C_{gd}. For the feedback loop, the PMOS transistor acts as a common-source amplifier thus a zero-cancelling resistor R_{gd} is required in series with the capacitance to ensure that the poles in the feedback do not fall into the right half-plane. This is depicted in Fig. 15b.



(a) *Feedforward path* (b) *Feedback path*

Figure 15: *Identifying feedforward (G(s)) and feedback (H(s)) transfer functions*

The transfer function G(s) for the feedforward path can be written as:

$$G(s) = \frac{g_m}{sC_L + \frac{1}{R_L}}, \tag{31}$$

since $R_{gd} >> R_L$ and $C_{gd} << C_L$. Thus we can identify the feedforward pole as:

$$p_L = -\frac{1}{R_L C_L}$$

For the feedback path, the required equations are:

$$V_{\text{amp out}} = A(s)\beta_R V_{in}$$
$$(A(s)\beta_R V_{in} - V_{out}) = g_m A(s)\beta_R V_{in},$$

which results in following transfer function:

$$H(s) = \frac{V_o}{V_i} = A(s)\beta_R \frac{sCgd + \frac{1}{Rgd} - g_m}{sCgd + 1/Rgd} \tag{33}$$

The positive zero can be cancelled with the feedback resistor, which should have a value corresponding $Rgd \leq 1/g_m$.

If the operational amplifier has a transfer function of the form of a two-stage opamp as in (24), it is safe to assume that the first pole is much lower than the differential amplifier's first pole. And since the load capacitance and resistance create a low pole in the loop gain G(s)H(s), the feedback path phase is most likely shifted 180° before UGB, causing instability.

To overcome this limitation, it is suggested to either 1) Lower GBW of the two-stage amplifier below system pole or 2) cancel the low-frequency pole created by the load or by the opamp. This can be performed by adding a small capacitor in the feedback path so that the open-loop feedback path will look like in Fig. 16.

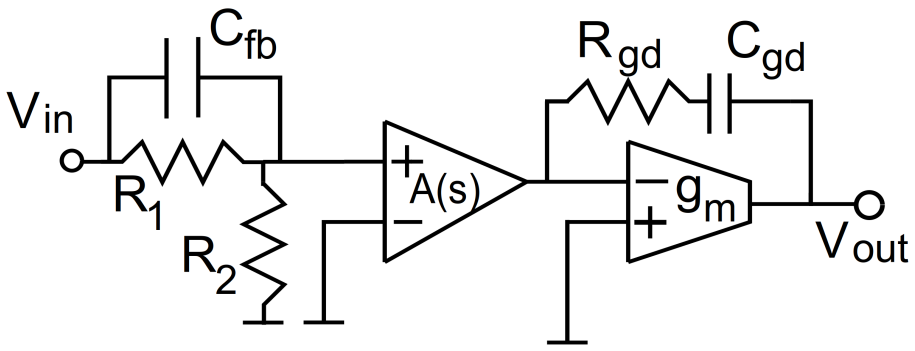


Figure 16: Adding a capacitor to feedback path

The voltage division between the parallel C_{fb} and R_1 with the series resistor R_2 is now:

$$V_+ = V_{in}\frac{R_2(sC_{fb}R_1+1)}{R_2(sC_{fb}R_1+1)+R_1}$$

Thus a negative zero and pole are created as:

$$z_{fb} = -\frac{1}{C_{fb}R_1} \qquad\qquad p_{fb} = -\frac{R_1+R_2}{C_{fb}R_1R_2}$$

The pole is higher than the zero so it will not affect the phase if correctly chosen. This zero can be used to cancel the second pole of the amplifier so that the effect of a double negative pole can be avoided.

Now the transfer function for the feedback path can be identified as:

$$H(s) = \frac{(1+\frac{s}{z_{fb}})(1+\frac{s}{z_{gd}})}{(1+\frac{s}{p_{fb}})(1+\frac{s}{p_{gd}})}A(s) \tag{35}$$

4.4.1 Full transfer function and root locus

Now that the system transfer functions G(s) and H(s) have been identified, the full negative feedback transfer function with a two-stage opamp is:

$$T(s) = \frac{G(s)}{1 + KG(s)H(s)} = \frac{\frac{g_m}{1+\frac{s}{pL}}}{1 + g_m A_{DC} \frac{(1+\frac{s}{z_0})}{(1+\frac{s}{p_0})(1+\frac{s}{p_1})} \cdot \frac{(1+\frac{s}{z_{fb}})(1+\frac{s}{z_{gd}})}{(1+\frac{s}{p_{fb}})(1+\frac{s}{p_{gd}})(1+\frac{s}{p_L})}} \tag{36}$$

Root-locus analysis can be used to obtain information how the loop transfer function KG(s)H(s) will behave as a function of loop gain K. K in (36) is $g_m A_{DC}$.If one is to modify the loop gain such that it is divided into numerator N(s) and denominator D(s), the denominator of (36) can be written as:

$$1 + KG(s)H(s) = D(s) + KN(s) \tag{37}$$

Now if the gain K of the feedback is very large so that $D(s) << KN(s)$, the zeroes of the loop gain become the poles of the system function (36). Root-locus analysis considers the behaviour of loop-gain poles and zeroes with varying K. If the loop gain has right half-plane zeroes, it is possible that large K will result in right-half plane poles for the system. One pole will create a locus with one zero and as K is ramped up, the pole will approach the corresponding zero. If the pole does not have a corresponding zero pair, the pole might enter the right half-plane and will become unstable. [34]

Both g_m and A_{DC} values can affect system instability but it should be more reasonable to set opamp gain as a varying parameter and set g_m as the highest possible value (maximum LDO operation range DC operation point and for this work $g_m = 2.7mS$ is used).To plot the stability as a function of opamp gain, it is required to normalize the loop gain $KG(s)H(s)$ by A_{DC} and plot the root locus of the loop gain.

In Fig. 17, the theoretical root-locus plot is presented. This system's loop gain has three zeroes and five poles, since a two-stage operational amplifier is modelled. One of the zeroes is very high and can be though as infinite and the fifth pole (highest) will go towards it (red locus). The second highest zero creates a locus with the fourth pole and it will stay in the left half-plane. The third pole and first zero create a locus and will also stay in the left half-plane.

The problem arises with the two lowest frequency poles. In Fig. 18, the low pole created by the load capacitance and resistance and the 2nd lowest pole created by the opamp, will enter the right half-plane at A_{DC} value of 453 (53 dB).

This section of this thesis has presented the functionality of the LDO first in DC operation and secondly in the AC operation, where a bandpass filter approximation for the LDO line regulation was derived. In the bandpass filter approximation, high gain amplifier with very high GBW is recommended along with the largest available load capacitor.

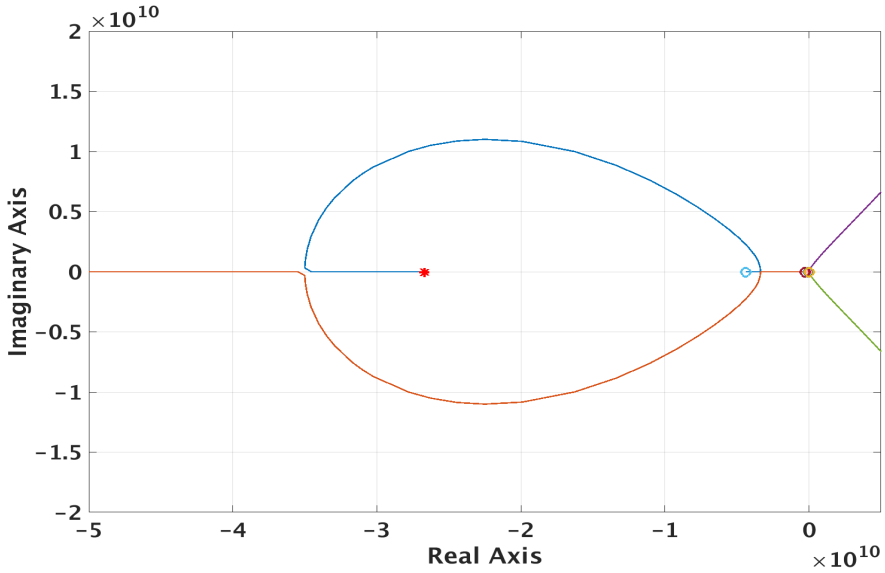


Figure 17: Root-locus of the theoretical loop gain with approximate values

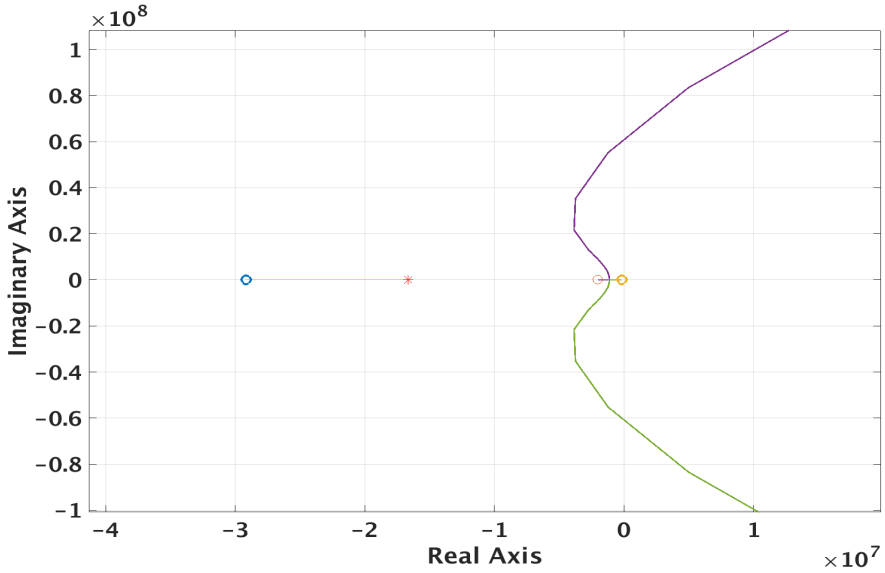


Figure 18: Two low frequency poles without corresponding zeroes can lead to instability

During simulations, it was found that using a two-stage operational amplifier in the LDO loop requires compensation methods and in the last part of this section two compensation methods were presented: 1) Gate-to-drain Miller-compensation with a zero-nulling resistor and 2) a feedback zero capacitor compensation that compensates for one of the poles in the feedback path.

Finally, a full negative feedback system function was written and a root-locus analysis was performed to identify a gain limitation approximation for the operational amplifier.

5 Implementation

In this section, the implementation of the separate parts of the system are presented and reviewed. First the pre-layout simulations are executed to evaluate the final performance of the system. After this, the layout is executed and the parasitics (RC or only C) are extracted so that the pre-layout simulations can be performed for the post-layout model as well.

5.1 Rectifier

This section describes the full implementation of the rectifier. A two stage rectifier is used and it's schematic is presented in Fig. 19. The added 2nd stage improves the output DC-voltage at the cost of PCE. The transistor's are named as $N/P_{stage,phase}$ to easily identify and extract the corresponding parameters of the desired transistor from the simulation results.

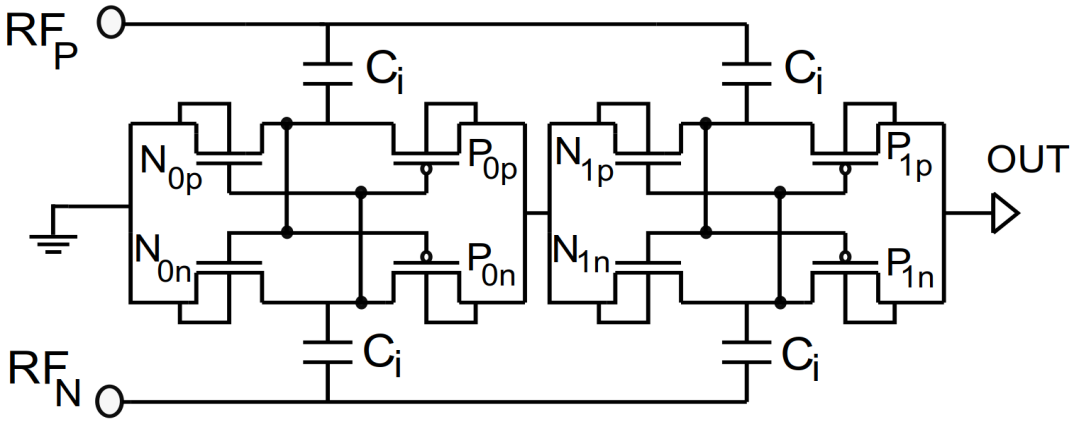


Figure 19: A two-stage rectifier

5.1.1 Pre-layout Simulations

The simulation setup is presented in Fig. 20. The matching components are denoted with m and input power is given as a magnitude of dBm.

The first stage in finding the optimal performance of the rectifier is to find the input matching for an arbitrary-, yet reasonable sized transistors by using the principles in section 3.1.2. A reasonable value for the channel width **W** of the NMOS is 2μm and PMOS is 6-10μm.The channel length **L** is kept at minimum.

The initial values are presented in Table 1 and the matching parameters are calculated by using the matching theory described earlier in section 3.1.2.

To verify the input matching, extract the differential voltage $RF_P - RF_N$ and current through the capacitors C_i in time domain. For the initial values, a transient simulation is presented with various values of input RF power.

To match the desired PCE, the close vicinity of 24 nH inductor value is varied and 28 nH inductor is chosen to accomodate the estimated power requirement. Finally

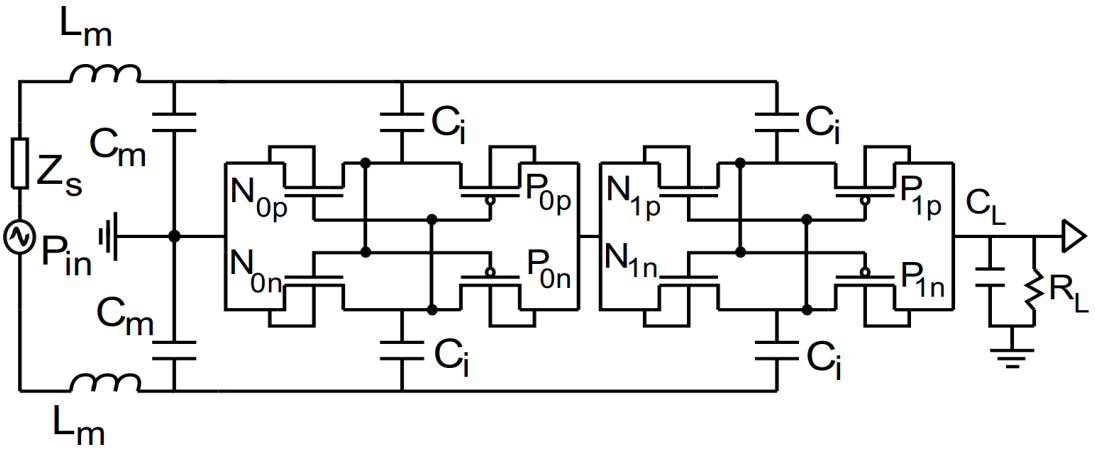
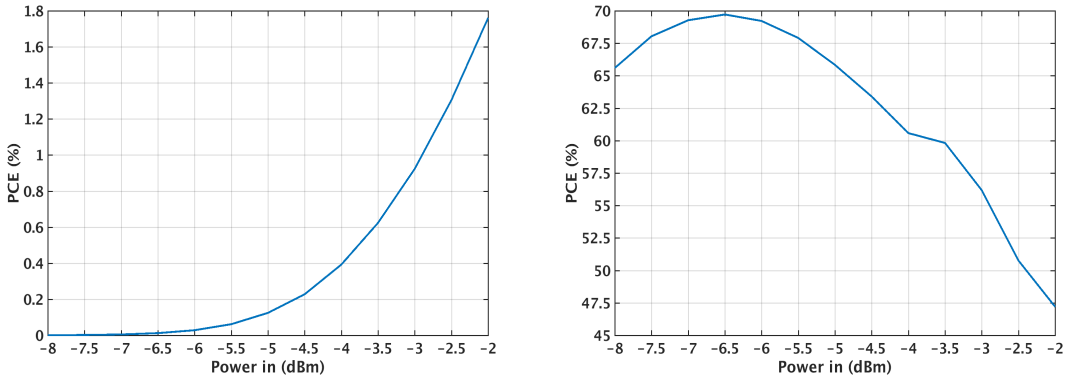


Figure 20: Simulation setup for the rectifier

C_i	500 fF	NMOS (w)	2 μm
C_m	900 fF	PMOS (w)	6 μm
C_L	1 pF	L_m	24 nH
f	860 MHz	R_L	5 kΩ
Z_s	100+j0 Ω		

Table 1: Initial values for the rectifier



(a) *Without matching* (b) *With matching*

Figure 21: *PCE with and without the proposed matching circuit*

match the transistor sizes by keeping W_n/W_p as constant. Final values of $W_n = 12\mu$ and $W_p = 48\mu$ are chosen, which yields the PCE-curves with different load resistor values presented in Fig. 22.

The load for this work is approximated as 5 kΩ as the LDO load will draw around 150 μA at 0.7 V. The PCE curves can also be adjusted by changing the ratio of W_n/W_p to adapt the desired requirements.

Generally the implementation of rectifier chip is measured directly without any matching procedures [35] and the matching for a mass-produced chip is performed either off-chip or after alpha/beta -stage testing have been verified [35]. The input

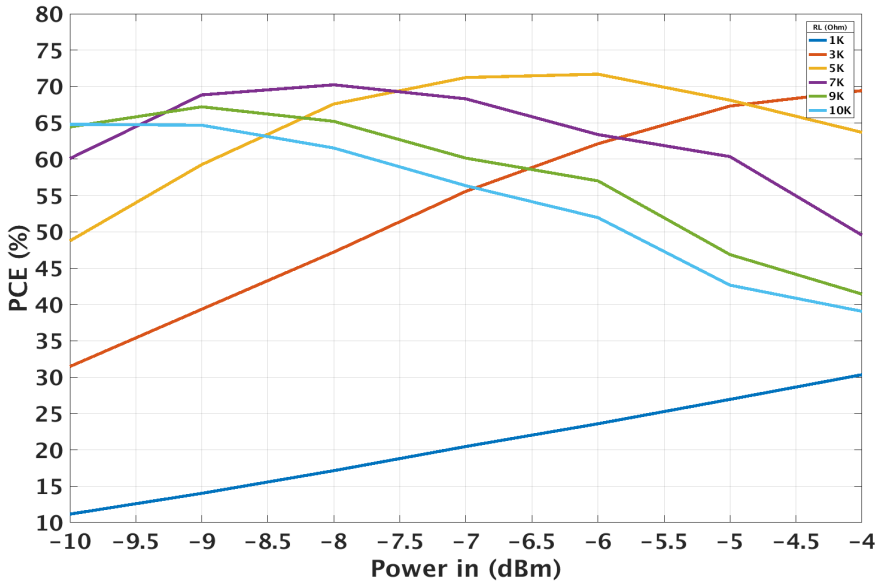


Figure 22: Load resistance's effect on PCE

impedance behaviour of an RFID chip can be divided into two stages: 1) Before 'Wakeup threshold' when the load is not drawing much current and 2) after 'Wakeup threshold' when the real part of the impedance starts to grow as a function of input impedance.

5.1.2 Layout and post-layout simulations

As the current drawn by the load is relatively large for modern small linewidth CMOS processes - the layout of the rectifier must take the possibility of generating too much heat inside the rectifier into account, since this can possibly destroy viable connections in the layout (via's). The layout in this work both matches the NMOS/PMOS -pairs inside the same well to achieve the best performance possible and uses wide metal lines to spread the heat stress evenly. The 2nd stage NMOS's bulk must be lifted to a triple-well design since the bulk is biased to the output of the first stage (see Fig. 19). The first step of the layout is to decide the position's of the transistor pairs. The input capacitors C_i will demand most of the area but they can be fairly well distributed to the surrounding area.

In Fig. 23 the layout for the rectifier is presented. the input capacitors (blue/orange metal lines) take most of the space. The 1st and the 2nd stage have somewhat of a separation due to the physical restrictions on the triple well required for the bulk connections (see again Fig. 19). In the triple well design, additional N-well must be created deep inside the p-substrate ('Deep N-Well') to isolate the main p-substrate from the newly created 'lifted p-substrate' region. Fig. 24 illustrates the idea behind shifting the bulk-bias with a triple well.

To verify the functionality of the layout, RC-parasitics are extracted from the layout to a separate file and the original simulations from previous section are then

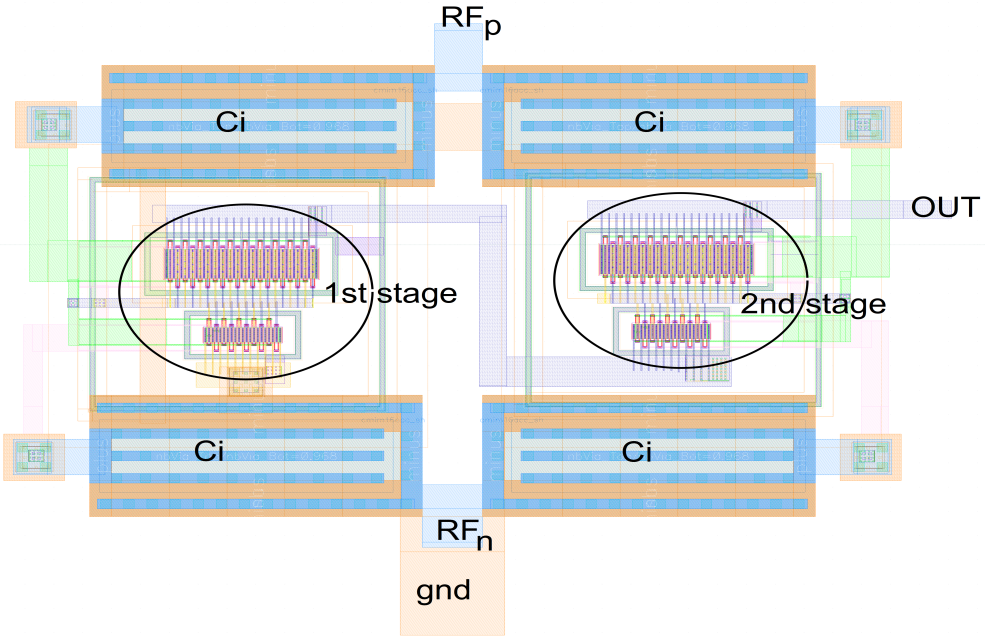


Figure 23: Rectifier layout

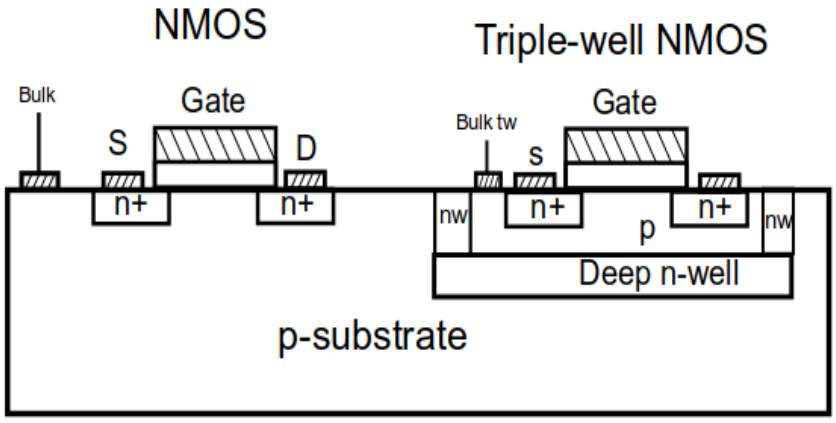
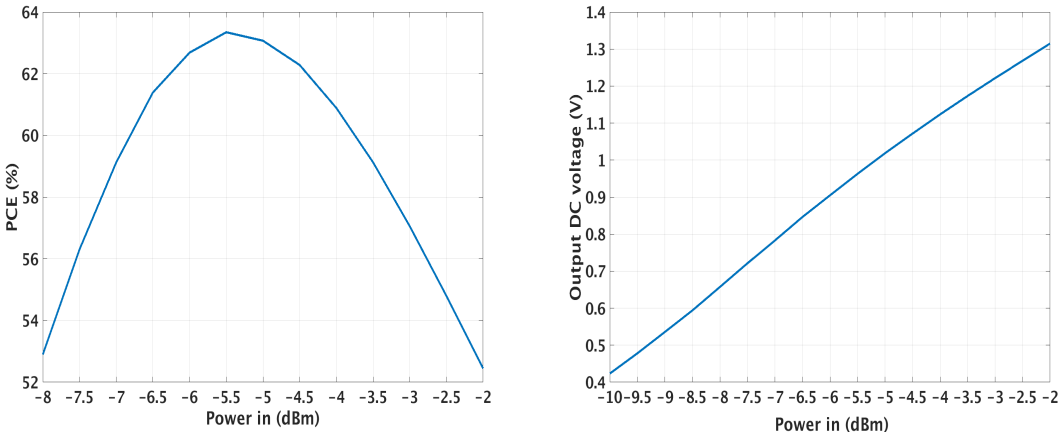


Figure 24: Triple well illustration

executed. Fig. 25a and 25b show the performance of the rectifier to a $5k\Omega$ load after layout. An approximate 7% difference in PCE is obtained, as the parasitics create mismatch between the matching components. The PCE peaks at -5.5 dBm input power at a value of 63%. The DC output level is 950 mV at the peak PCE input power. In section 2 the effect of IC-inductor non-idealities were briefly discussed, and it would be safe to assume a significant reduction in PCE value using non-ideal inductor models, depending on the chosen inductor.



(a) *Post-layout PCE* (b) *Post-layout DC level*

Figure 25: *Post-layout PCE and DC-level performance*

5.2 Reference circuitry

The design of the reference circuitry for the LDO follows the Betamultiplier (BMR) design presented in [36]. In a BMR circuit, an NMOS current mirror forced to maintain a constant current trough the biasing resistor R. An added PMOS current mirror is connected to the drain of the mirror side NMOS N2 to force the current through N2 through P1. The fundamental idea is presented in Fig. 26.

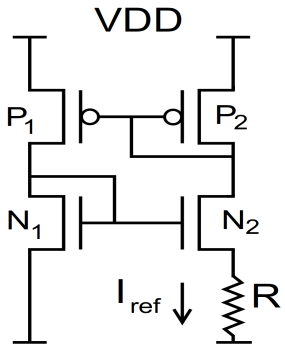


Figure 26: Development of BMR

The gate-to-common voltages must be equal:

$$V_{gs1} = V_{gs2} + I_{Ref}R$$

From this we will acquire:

$$\sqrt{\frac{2I_{Ref}}{\beta_1}} + V_{TN} = \sqrt{\frac{2I_{Ref}}{\beta_2}} + V_{TN} + I_{Ref}R \tag{38}$$

Where $\beta = KP_n\frac{W}{L}$ and V_{TN} the threshold voltage of NMOS. And $\beta_1 = K\beta_2$, thus the name Betamultiplier. In this structure, I_{ref} and V_{gs1} will remain constant. From (38) it is possible to write the equations from which the references are calculated:

$$I_{Ref} = I_{dn1} = \frac{2}{\beta_1 R^2}(1 - \frac{1}{\sqrt{K}})^2 \tag{39a}$$

$$V_{Ref} = V_{gs_1} = \sqrt{\frac{2I_{Ref}}{\beta_1}} + V_{TN} \tag{39b}$$

This simple structure is not enough to function as a reliable reference. While being less sensitive to supply voltage change, the current will still increase since if VDD goes high, the V_{SG} of PMOS will increase.

To further decrease sensitivity to supply, an opamp is added as in Fig. 27a to hold the PMOS's V_{SG} constant. In this design, the opamp will keep drain of N2 and N1 equal to each other. If drain of N2 goes high, the opamp output will go high, reducing the current going through N2. Because of the current mirror connection, the current in the left side (N1) is also reduced until both currents are equal. The main limiting factor in this implementation is the matching of the MOSFET sizes - which, if not correctly chosen, limit the gain and speed performance of the opamp. If the sizes are not matched, the PMOS N_{op1} and N_{op2} can load the BMR. The added NMOS N_{op2} is to ensure that the reference current also biases the operational amplifier so that the current drawn by the opamp is not linearly depended on VDD.

In Fig. 27b the added startup circuitry is to ensure the correct operation point for the gates of P1/P2 and N1/N2. If the gate of N1/N2 is at ground and P1/P2 is at VDD, then the gate of NSU2 is at ground. Therefore its source is at VDD - V_{THP} meaning that NSU1 can leak current between the gates of P1/P2 and N1/N2 until it is turned off. The added capacitors C_p and C_n are to ensure stable operation by reducing oscillations in the reference nodes. The final sizes of the transistors are presented in Table 2.

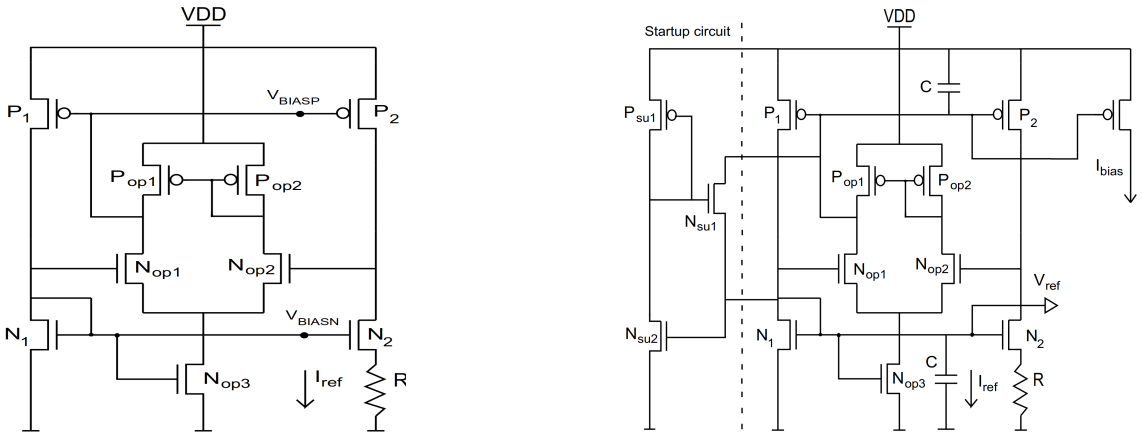
The equations (39a) and (39b) are for transistors operating in the saturation region. Since the desired reference is 400mV, it is below V_{th} and the resistor value required would be well above $M\Omega$ magnitude. Subthreshold operation equation from [36] is given as:

$$R = \frac{nV_T}{I_{Ref}} ln(K) \tag{40}$$

where V_T is the thermal voltage kT/q (approximately 25.3 mV) and $n = 1 + C_D/C_{ox} \approx 1$ [16]

5.2.1 Implementation

The design of the BMR starts with choosing the standard β value of 4. The general width of the NMOS N1 is chosen to be 2 μm, therefore $W_{N2} = 8\mu m$. With (40) the



(a) *Betamultiplier with an opamp* (b) *Final reference circuitry*

Figure 27: *Final reference circuitry*

resistor value is approximately $350k\Omega$. The PMOS width is chosen to be $2 * W_n$. Gate length should be increased to at least 150 nm to increase the voltage and output impedance. These values should be used for the opamp MOSFETS $Nop_{1,2}$ and $Pop_{1,2,}$ as well to maintain the correct matching.

Simulations indicate the optimal resistor value to be 400 kΩ and the NMOS gate length has been raised to 440 nm to increase V_{gs1}. PMOS gate length is set to 300 nm. Results obtained are presented in Fig. 30. PSRR is measured as the difference V_{Ref}/V_{Vdd} and the relationship between the VDD operation DC-range and PSRR can be seen clearly which is the operation range of the opamp.

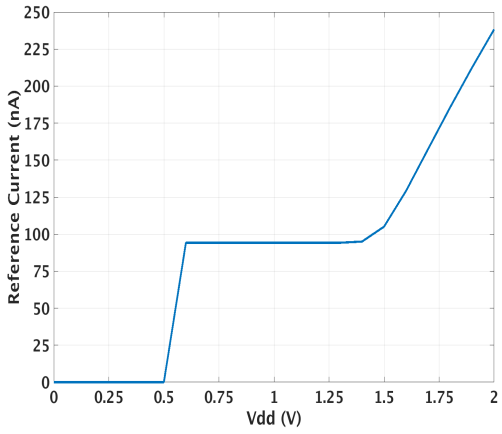
$N_{1,op1,op2,su2}$	$\frac{2\mu}{400n}$
N_2	$\frac{8\mu}{400n}$
$P_{1,2,op1,op2}$	$\frac{4\mu}{300n}$
N_{su1}	$\frac{80n}{200n}$
P_{su}	$\frac{160n}{400n}$
$C_{n,p}$	500 fF
R	$400k\Omega$

Table 2: Reference circuitry part values

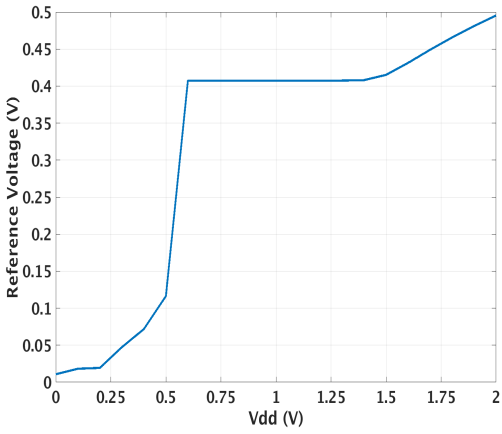
Should the design require a higher operating region and more stable reference with respect to VDD, a cascode structure is recommended to work as an output buffer. By this method, the output resistance can be increased drastically and the opamp inside the betamultiplier can be calibrated to work in a more wide region of VDD.

5.3 Operational Amplifier

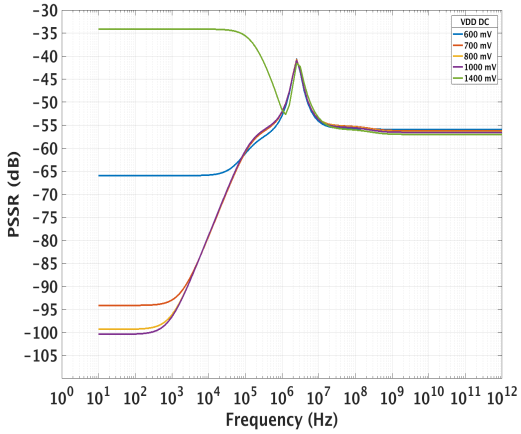
A single-stage differential amplifier is chosen for this work due to the ease of implementation with the LDO structure: No compensation is required and the gain



(a) *Reference current*



(b) *Reference voltage*



(c) *BMR PSRR*

Figure 28: *Reference circuitry performance*

bandwidth (GBW) is high with low total current consumption.

Initially, the digital circuitry of the load was designed to work in 500 mV, forcing the reference circuitry to provide a 400mV reference for the LDO. The threshold voltage V_{th} for this design kit is 470mV, forcing the input NMOS transistors to operate in subthreshold region, which limits the available DC gain of the opamp. The load capacitance due to LDO PMOS transistor is estimated to be in 200-500 fF range.

The design goals are presented in Table 3. To maximize the GBW, the NMOS gate length is kept small at $W/L = 32\mu/60n$. This sacrifices DC gain but the importance of the large first pole shown in section 4 was prioritized. The current mirror load size is set at $W/L = 8\mu/80n$, which achieves a 28 dB DC gain, with a 14 MHz GBW to 500fF load. The opamp dissipates approximately $1.5\mu A$ with a mirroring ratio of 16 with respect to the reference current. The open-loop gain performance is shown in Fig. 30a.

For the PMOS load, a very large ($W/L = 200\mu/150n$) transistor was chosen.

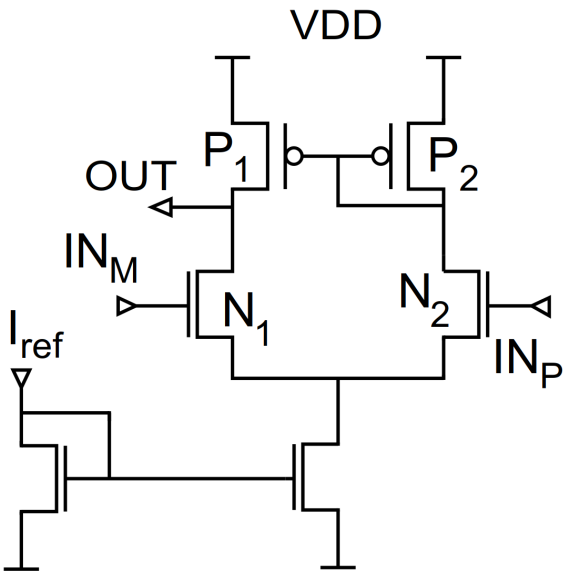
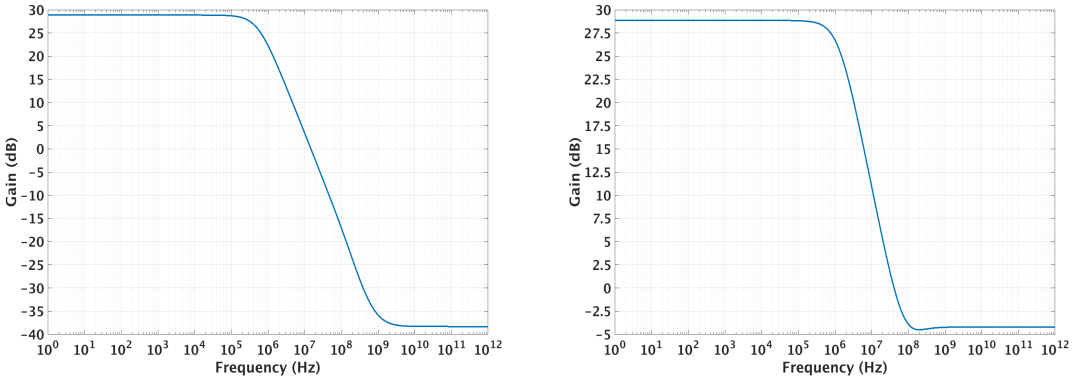


Figure 29: Differential amplifier schematic

VDD	0.7 V
Gain	Maximize
GBW	Over 10 MHz
PSRR	Unspecified/Maximize

Table 3: Opamp design goals



(a) *Driving a 500fF capacitor* (b) *Driving a very large PMOS transistor*

Figure 30: *Differential amplifier driving capability*

150 nm is the minimum gate length for high V_{ds} FET's which in turn raises the dropout voltage of the LDO. For this large transistor, the 500 fF load capacitor in the open-loop simulation was too much, and as can be seen from Fig. 30b, the pole is 1.25MHz and the GBW for this load is 40 MHz which leaves enough headroom for an oscillating load. The final specifications are listed in Table 4.

VDD	0.7 V
Gain	28 dB
GBW	Over 35 MHz @ 300 fF
Current Consumption	$\approx 1.5\mu A$
PSRR	27 dB @ 860 MHz (70 dB @ DC)
Phase Margin	>70°
CMRR @ DC	64 dB @ DC and 6 dB at UHF
ICMR	0.25-0.5 V
VDD operation range	0.6-2.5 V

Table 4: Differential Amplifier Specifications

5.3.1 Two-Stage Miller-compensated Operational Amplifier

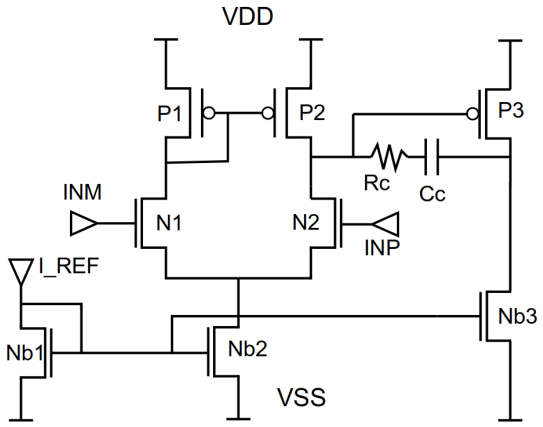


Figure 31: Two-stage opamp schematic

Initially a two-stage Miller-compensated opamp was designed to operate at 500 mV VDD, but later to the design the supply voltage was relaxed to 700 mV.

Most of the design guidance is taken from [37] which describes low-supply sub-threshold design for a two-stage Miller compensated amplifier. Generally it is first recommended to start by optimizing the first stage gain and bandwidth ratio which are depended largely on 1) input DC bias current 2) input transistor g_m/g_{ds} ratio and PMOS current mirror load g_{ds}. Conveniently, the previously presented single-stage opamp can be used as a basis for the two-stage opamp, but it might not be entirely compatible with the following common-source stage.

When the first stage is optimized, the compensation capacitor size can be calculated from the desired GBW as in (41) [37],[33]. With input MOSFET transconductance g_{m1} of $24\mu S$ and a desired GBW of over 20 MHz, the compensation capacitor would be 200 fF.

$$C_c = \frac{gm_{n1}}{2\pi GBW} \tag{41}$$

As the load capacitance was approximated to be 300fF, the second pole occurence can be approximated to be:

$$f_{sp} = \frac{gm_{p3}}{2\pi CL} \text{ [38]},$$

which yields 32 MHz for a PMOS transconductance of $60\mu S$. The desired phase margin (60°), GBW and second pole have a relation of the following:

$$tan(PM_{rad}) = K = \frac{f_{sp}}{f_{GBW}} \text{ [38]}.$$

This yields a phase margin of 57°. The compensation resistance can be calculated via the desired phase margin with (42) [37].

$$R_c = \frac{1}{2gm_{p3}}(1 + \sqrt{1 + \frac{4gm_{p3}C_L}{gm_{n1}C_1 tan(PM)}}), \tag{42}$$

where gm_{p3} is the transconductance of the output PMOS and C_1 the full parasitic capacitance in the output node 'PM' is the desired phase margin in radians.

Fig. 32 shows the performance to 300 fF load capacitance. The DC gain is 60.67 dB with the first pole located in 31 kHz. The GBW is 31 MHz. The phase margin is 56°, so it matches very well with the theory. The specifications for the initial design are listed in Table 5 (to 300 fF load).

VDD	0.7 V
Gain	60 dB
GBW	31 MHz @ 300 fF
Cc	200 fF
Rc	40 kΩ
Current Consumption	$\approx 6\mu A$ (1.5+4.5 μA)
PSRR	27 dB @ 860 MHz (51 dB @ DC)
Phase Margin	56°
ICMR	350-600m @ 0.7 VDD
CMRR @ DC	68 dB

Table 5: Two-Stage opamp specifications

The PSRR is measured as $PSRR^+$ (positive supply variation), where the supply VDD is set to fluctuate and the opamp is configured in unity gain configuration (INM shorted to OUT).

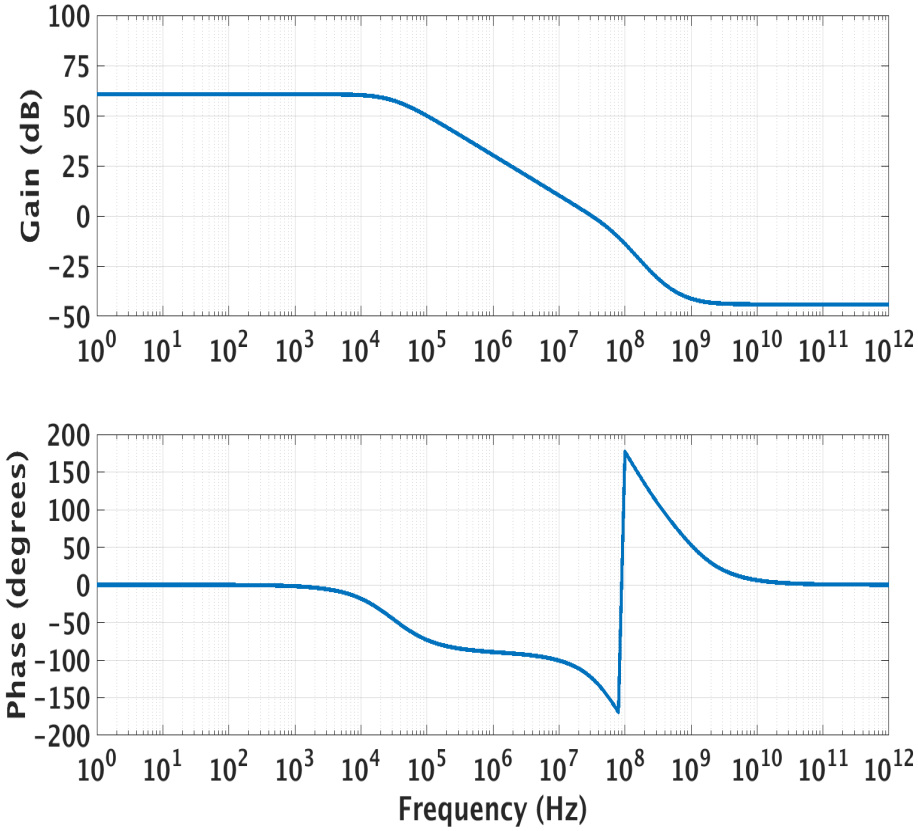


Figure 32: Initial two-stage opamp performance

Even if the opamp is unity-gain stable with the initial design, the phase margin is not enough for the opamp alone to be stable in the LDO loop due 1) LDO PMOS transconductance stage and 2) additional poles created by LDO loop gain.

Phase margin can be increased to 90° with $Cc = 1.8p$ and $Rc = 21k\Omega$. With these values, the first pole of the opamp is created in 4 kHz and the GBW is diminished subsequently to 4 MHz. The open-loop performance can be seen from Fig. 33.

While this increased phase margin would be enough to work in the LDO feedback loop; the first pole, which determines LDO's first zero, is very low and thus diminishes performance of the LDO. It is suggested to use the compensation methods presented in subsection 4.4 that allows the use of higher GBW opamp.

5.4 LDO simulations

After the opamp and reference circuitry performance are evaluated, both are simulated fully in the LDO configuration. A voltage source is set to oscillate at the input with a DC-value, which will be ramped up in the DC-simulations to obtain the operation range of the LDO. The stability of the loop can finally be obtained with time domain transient regulation results (both load- and line transient). All the results presented in this section are simulated **with the reference circuitry**, however it is first

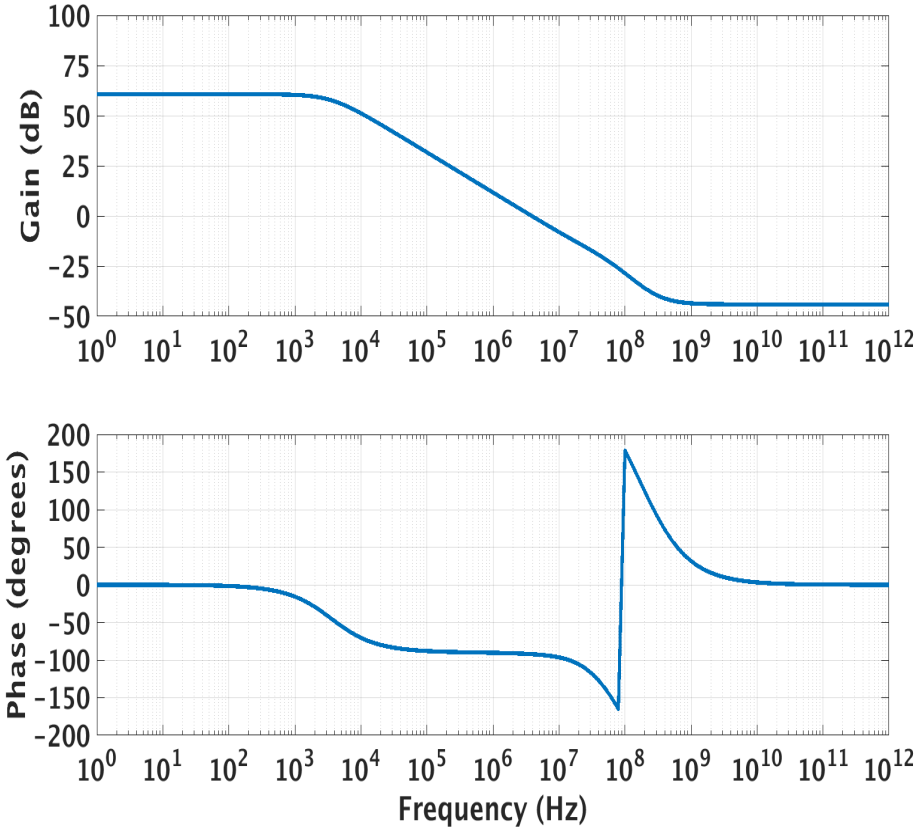


Figure 33: Increased phase margin opamp performance

convenient to use required ideal voltage- and a current sources and add the designed reference circuit later on.

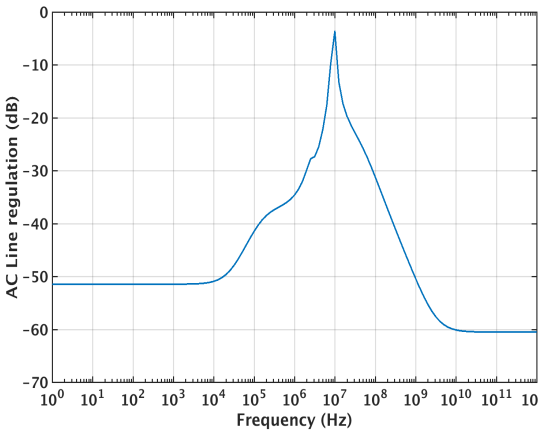
5.4.1 Differential amplifier

The line regulation is given in 34a. The DC line regulation is 53 dB @ 1.2 V with the worst value of -3.6 dB at 10 MHz. The load capacitance is set at 50 pF. The DC operation range is shown in Fig. 34b and ±1% output voltage range is 0.755-1.405 volts, which is sufficient given the rectifier DC performance.

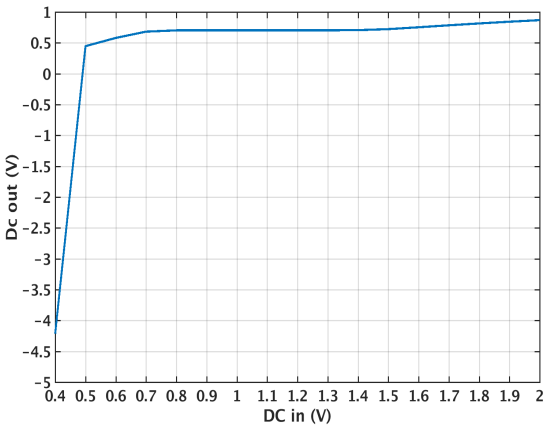
To verify loop stability, an input voltage transient and output current transient are introduced separately. The settling time for an input transient is approximately $5\mu s$ with a transient voltage regulation of 0.5/100 mV.

The load transient setting time is approximately $3.5\mu s$ with a transient voltage regulation of 8mV/300 nA. Results are presented in Fig. 36. The output referred noise is below $80\mu V/\sqrt{Hz}$ @ DC and $1\mu V/\sqrt{Hz}$ @ 10 MHz using the real component models. The noise is relatively constant within the LDO operation range but will yield higher values after the breakdown voltage at approximately 1.4 V. The PSRR at UHF band is measured being over 74 dB.

In section 4 the transfer function for the LDO loop was presented. While not

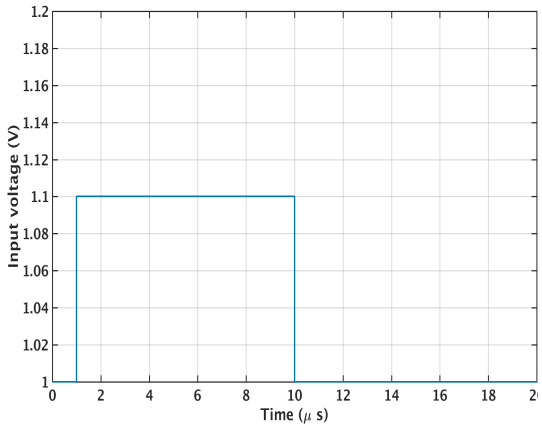


(a) *Pre-layout line regulation*

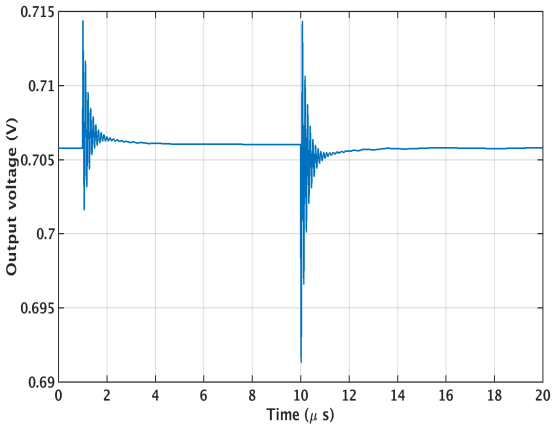


(b) *Pre-layout DC operation range*

Figure 34: *Pre-layout input transient simulation*



(a) *Input transient voltage*



(b) *Output voltage settling*

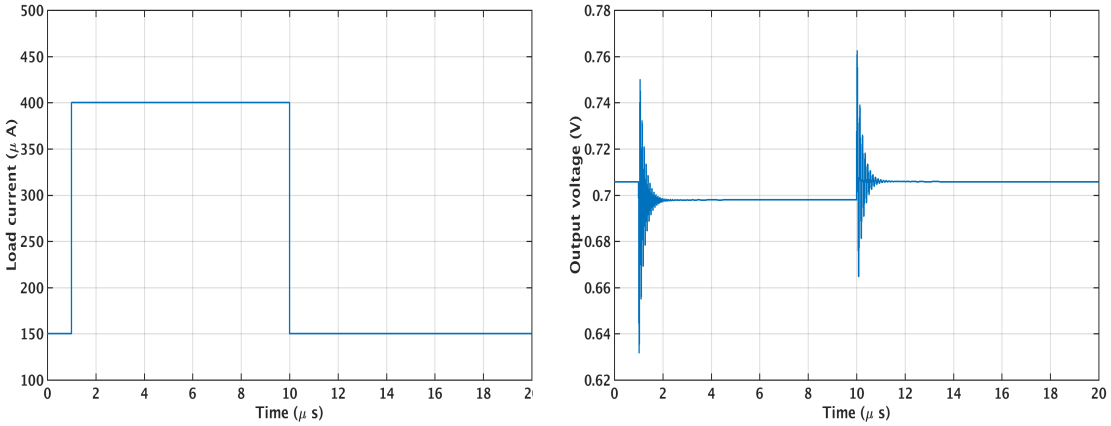
Figure 35: *Pre-layout input transient simulation*

all parameters can be changed during the pre-layout simulations, capacitance can be added easily and the size of the transistor can be scaled. Fig. 37 shows how the added capacitance at opamp output (lowering the pole) shifts the line regulation resonance frequency lower and increases the gain of the system as was predicted by (20).

The LDO load capacitance behaves as predicted by (20): More capacitance shifts the resonance frequency lower and increases line regulation performance in the circuit. The load capacitance effect is presented in Fig. 38.

5.4.2 Two-Stage Operational Amplifier

The two-stage operational amplifier is simulated, but not implemented on layout due to questionable power consumption and line regulation performance.



(a) *Output transient current* (b) *Output voltage settling*

Figure 36: *Post-layout output transient simulation*

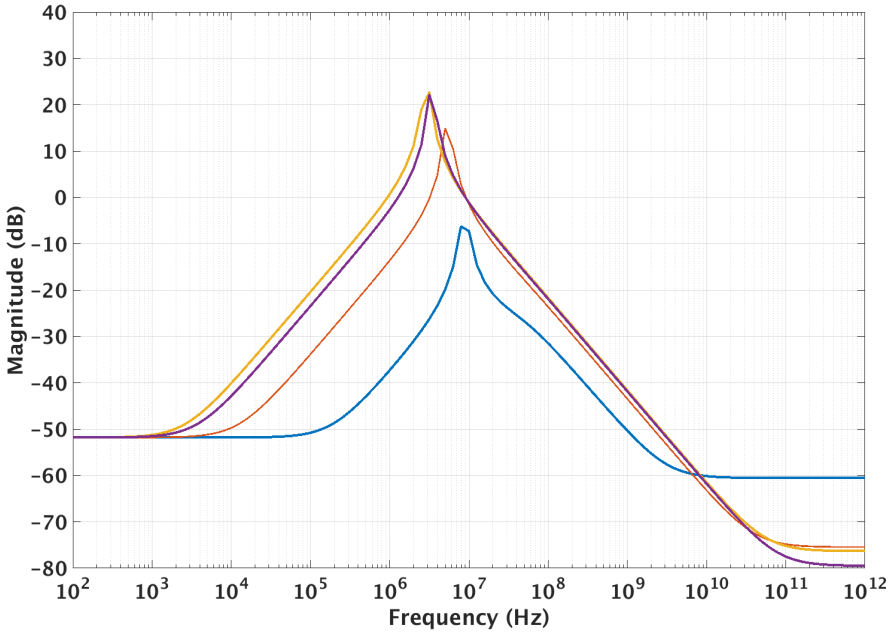


Figure 37: Decreasing the pole of opamp by adding capacitance at opamp output

Without the compensation scheme presented in subsection 4.4, the unstable line regulation magnitude and phase performance can be seen from Fig. 39a and 39b and the system was verified to be unstable with transient simulations, where the same impulses as in 35a and 36a were used.

To overcome this problem, pole-splitting capacitor C_{gd}=90f and a zero-cancellation resistor $R_{gd} = 45k\Omega$ is placed between gate and LDO output and a feedback network zero is added with a capacitor C_{fb}=200f. The function of $C_{gd} = 100fF$ is to increase phase margin at feedback path and R_{gd} is to cancel the positive zero created by pass PMOS transistor transconductance g_m zero.

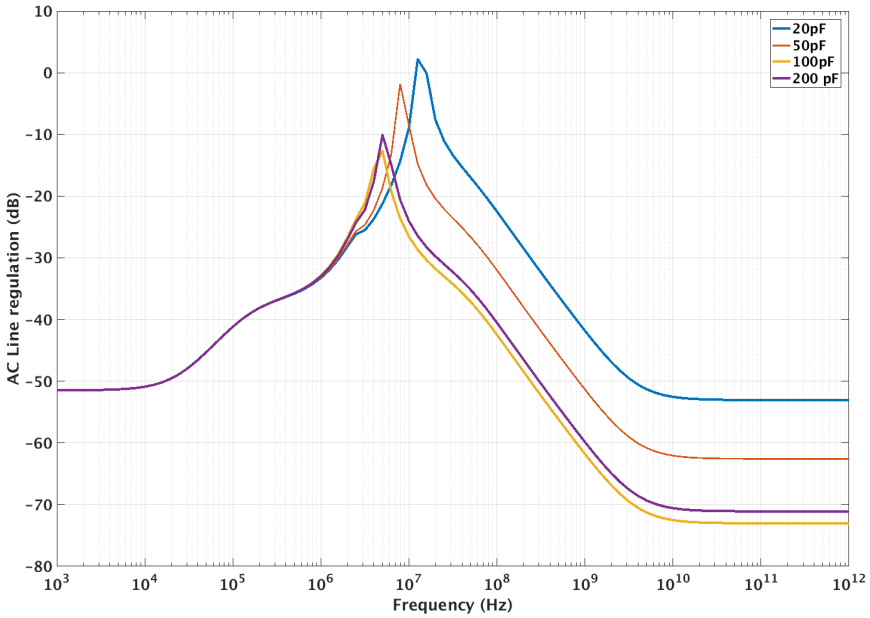
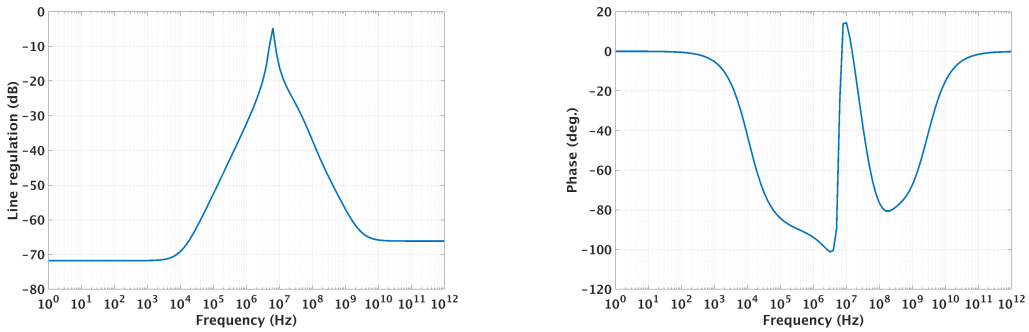


Figure 38: Increasing load capacitance



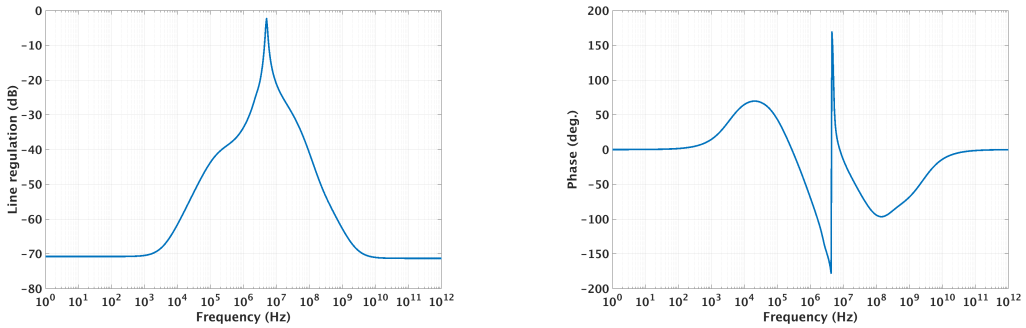
(a) *Unstable magnitude response* (b) *Unstable phase response*

Figure 39: *Unstable line regulation with two-stage opamp*

With these components, the line regulation can be made stable and results are shown in Fig. 40.

The load regulation is measured with $150\mu A$ DC current value and it achieves a 1Ω value at DC due to high gain of the amplifier but forms a strong unwanted resonant peak right at center frequency. In Fig. 41 AC load regulation performance is evaluated.

The simulated input and output transient excitations are shown in Fig. 44. The feedback compensation capacitor can be increased to decrease settling time but it's size is limited due to the pole it also creates.



(a) *Stable magnitude response* (b) *Stable phase response*

Figure 40: *Stable line regulation with two-stage opamp*

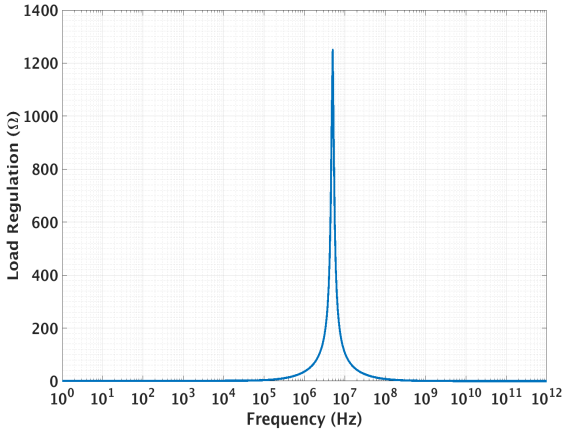
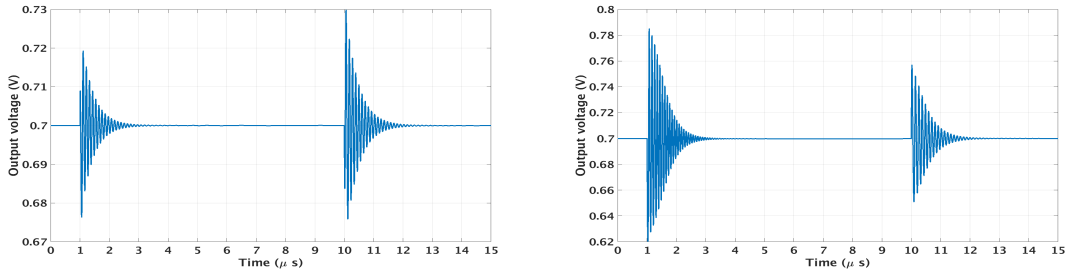


Figure 41: Load regulation with two-stage opamp at 150 μA DC load current. The DC load regulation value is 1.16Ω



(a) *Input transient response* (b) *Output transient response*

Figure 42: *Transient response with two-stage opamp and compensation network*

The input and output transient ringing times are comparable to differential amplifier performance, however the output DC voltage is not shifted as much with the two-stage opamp due to higher DC-gain. The output DC range is identical to differential amplifier because it is limited by the reference voltage, not the amplifier itself.

5.4.3 Post-layout verification

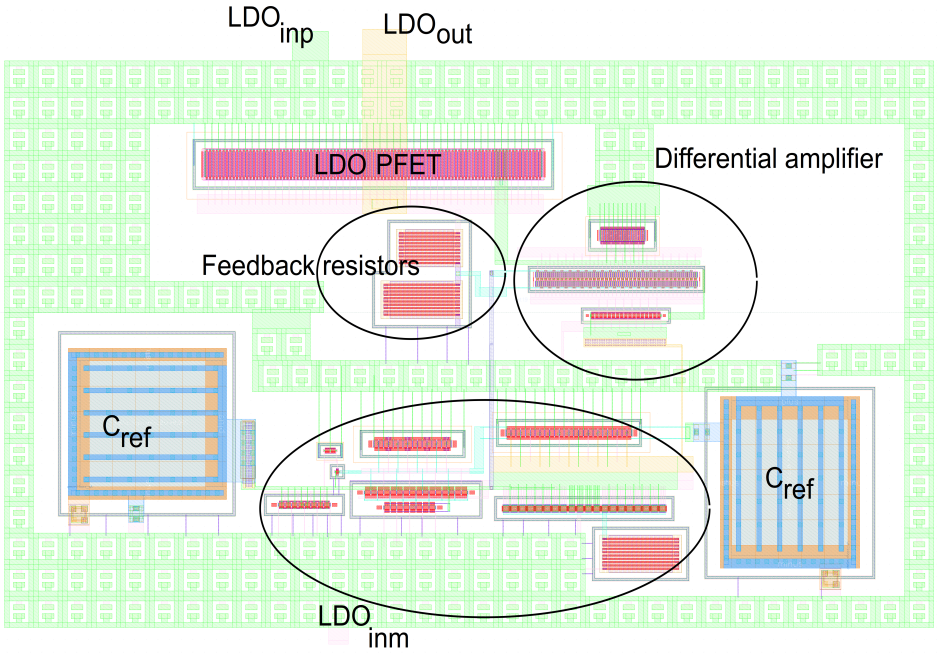


Figure 43: LDO layout

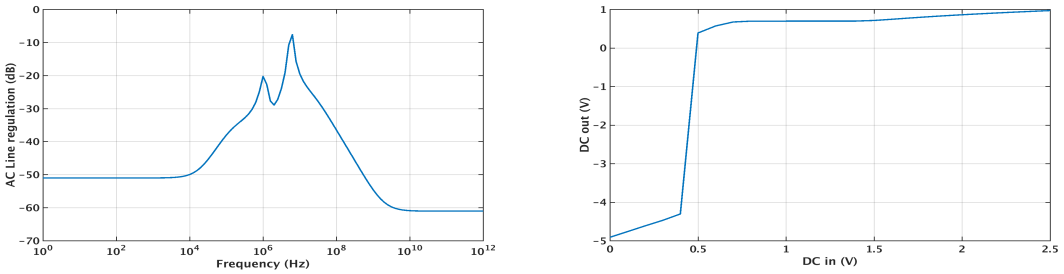
The layouts for the LDO parts (opamp, reference) are first implemented separately and then put together as shown in Fig. 43. All the transistor pairs are matched within the same well and the excess space is filled with a metal "Mesh" where the negative supply VSS can be supplied with uneven metal layers 1 and 3 and positive supply can be supplied with even layers 2 and 4. This Mesh can be seen as the green blocks surrounding the main parts in the layout. For the post-layout simulations only the capacitor extraction is made, since the simulation times with RC-extraction would be very cumbersome.

The reference circuitry layout is constructed so that the startup circuitry transistors are lie the leftmost, operational amplifier in the middle and the main BMR transistors on the right. The reference resistor lies "below" the BMR transistors. The reference stabilizing capacitors *Cref* take a lot of space and their position must be considered.

The operational amplifier layout is implemented as in the schematic (Fig. 29): Current mirror on the bottom, input transistors in the middle and load transistor lie uppermost.

For the full LDO, the load capacitance is increased to 100 pF so that line regulation is remains below 0 dB at all operation corners. The added capacitance(s) due to layout add another peak to lower frequencies. The dominant pole is shifted to a lower frequency which affects the largest peak. The peak is shifted from 10 MHz to 8.5 MHz and it's value is -7 dB due to the added capacitance. And due to these parasitics, the load transient response settling time is increased to over $6\mu s$ with a regulation level of $8mV/300\mu A$. Input transient response settling time is 5 μs and

regulation of 0.8/100 mV. The line regulation performance in typical corner at 1V input voltage is shown in Fig. 44a and the DC operation range in Fig. 44b.



(a) *Post-layout line regulation @ 1V input* (b) *Post-layout operation range*

Figure 44: *Typical corner post-layout performance*

A set of Monte-Carlo simulations are run for the LDO in the typical, slow and fast corners (FET's, capacitors and resistors) with an input voltage of 1 V. In the typical corner, the mean DC line regulation is -50.61 dB and output mean DC voltage 697 mV.

In the slow corner, the line regulation achieves a -50.6 mean DC value. For the output DC voltage, the resistor mismatch slightly increases the output mean value of 714 mV. Output referred noise stays below -80 dB for the whole band.

In the fastest available corner, the line regulation does not differ much; the peak shifts to higher frequencies and the mean DC line regulation is -51 dB. The mean DC output value is 690 mV. A single Monte-Carlo variation can create a peak of +0.5 dB in 6 MHz during worst-case corner, but the overall mean minimum line regulation value is below -5 dB.

5.5 Full chain layout and simulations

The rectifier and the LDO as a top-level layout are implemented on a 200x140 μm^2 area reserved from the top-left corner of the chip. The added inputs VDD and LDO_{in} and output LDO_{out} have been added for measurement purposes so that each part can be measured separately. The LDO input can be switched between the rectifier output or the external *vdd* input. The digital switching signals (top right) are routed from the digital part of the chip to control the switches properly.

The empty space can be filled with the external capacitance as *Meshcap* which consists of layers of metal in the upper layers and gate-source shorted FET-based capacitors in the lower layer. Such structure provides over 600 fF of capacitance in a 10 μm^2 area and can be implemented easily without excess bulk biasing. Note that in the chip implementation the load capacitance was left out to optimize the required capacitance in the measurements.

The circuit startup time is depended on input power and reference current startup time which controls the opamp loop configuration time. The startup time is in the range of μs. With the minimum input power -6.8 dBm (208 μW), the startup time is 42μs. This would mean that about half of the power is used by the rectifier

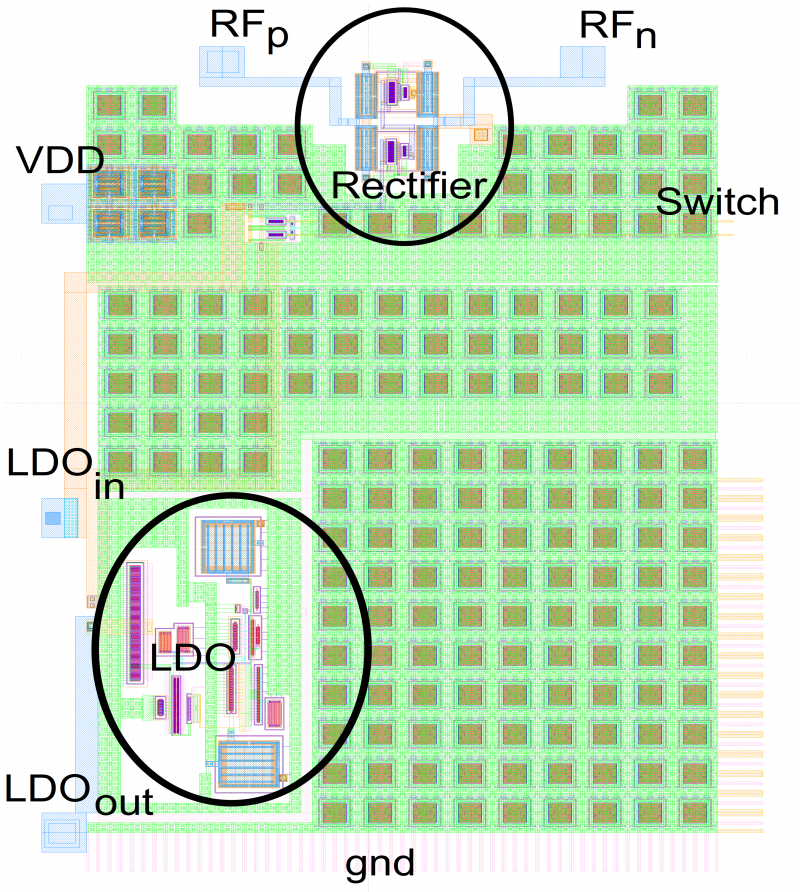


Figure 45: Power top layout

and LDO and another half by the load. The output ripple is depended on input power and at low input power (< 6.5dBm) it is less than 0.1mV. The transient simulation results are limited for the whole system since the post-layout model is very cumbersome and the transient simulation files are very large.

The breakpoint for the full-chain is approximately -2.4 dBm input power ($580\mu W$), when the input mean DC voltage exceeds 1.4 V. With -2.4 dBm input power the output peak-to-peak stays at 10 mV which can still be considered usable, however at -2.2 dBm input the output oscillations have a peak-to-peak value of 80 mV and at -2 dBm it is already over 100 mV. The effect of input power variation to the startup time can be seen from Fig. 46.

Transient Monte-Carlo simulations are also executed with both typical corner and slow corner using the minimum input power value (-6.8 dBm). The circuit operates with the typical corner worst-case scenario, however the startup time is significantly increased to over 60μs. In the slow corner (for FET's and capacitors), the circuit fails to achieve 700mV within the duration of 60μs.

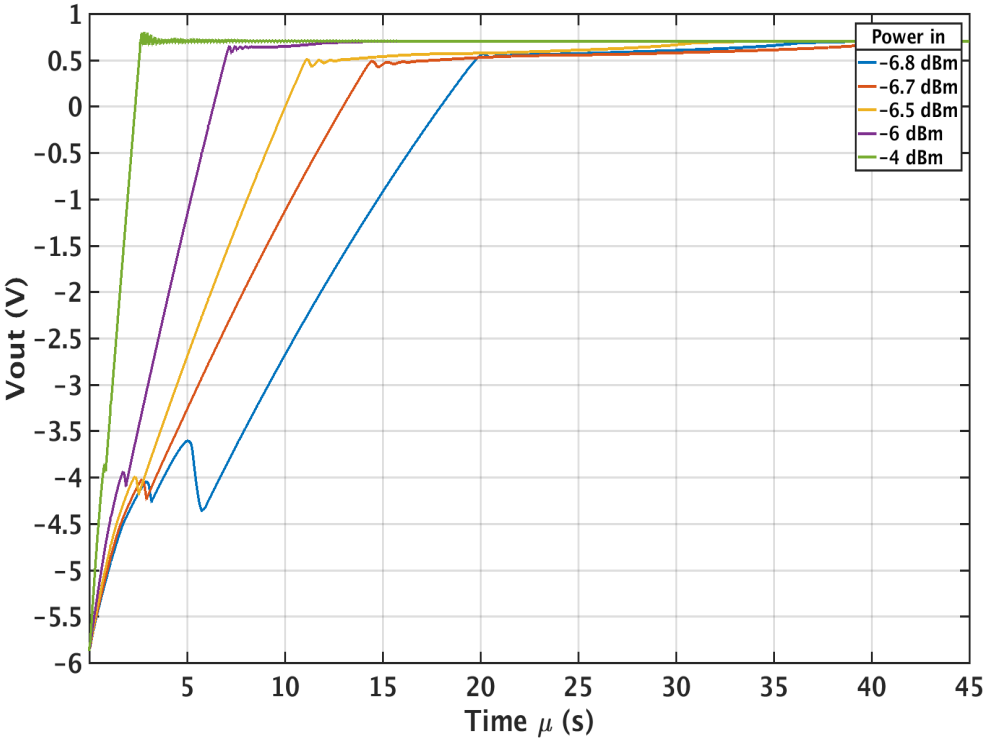


Figure 46: Power top transient simulation in typical operation corner

6 Conclusions

A fully-functioning RFID power system for neural signal acquisition has been implemented and its performance evaluated. The design was carried from theory to circuit level design and finally to layout. The theory part included fundamental circuit theory and Laplace-domain (s-domain) analysis. The rectifier and its impedance matching to a perfect power source was implemented as the two-stage cross-coupled bridge rectifier, with the performance evaluated both pre- and post-layout.

The rectifier operates as intended and it achieves a 63% peak PCE performance with -5.5 dBm input power. The input impedance matching was implemented with the theory presented in section 3 with a series inductor and a parallel capacitor. The sizing of the transistors started with an approximation based on other works and later optimized with the simulator to obtain the desired results.

To reduce all unwanted oscillations, the Low-Dropout Regulator requires a very high-bandwidth, high-gain operational amplifier that has high power supply suppression. Particularly this becomes a difficult challenge with subthreshold operation as the transistors have limited speed-to-gain ratio [36]. Due to the limited opamp performance, the LDO output capacitor is required to be very large, requiring a lot of surface area. The output DC voltage was initially designed to generate 0.5 V DC voltage but it was changed into 0.7 V later into this work due to the load circuitry specifications. Initially a two-stage opamp was designed for low-supply operation but power consumption and line regulation performance became a conflicting factor.

The reference voltage and -current for the opamp was designed with the *Beta-multiplier* -architecture with the principles of [36]. The reference voltage was set at 400 mV and reference current at 100 nA. The full DC current consumption of the reference circuitry and LDO opamp is approximately $2.3\mu A$ of which the opamp consumes $1.5\mu A$.

The complete final chain works with minimum input power of -6.8 dBm with a startup time of $42\mu s$. The power loss is mainly due to impedance matching, added switches and LDO dropout voltage. The complete design was implemented on a chip. For extremely low-power rectifiers, it is suggested to consider HTFET's (Hetetojunction Tunnel FET) which are capable of -33 dBm ($\approx 0.5\ \mu W$) input power sensitivity.

In the LDO design the noise produced by the reference is not a critical parameter since any unwanted oscillations in the reference supply are minimized with the stabilizing capacitors inside the BMR. The line-regulation s-domain analysis presented in section 4 gives a reasonable approximation for the system performance using a differential amplifier, however along with underestimated capacitance, there are missing zeroes and poles to give a more appropriate behavioural analysis.

Along with the differential amplifier, the performance was evaluated with the two-stage Miller compensated operational amplifier. Due to phase performance, compensation methods should be taken into use when used in the LDO feedback loop. If not compensated properly, the phase margin at the opamp output, when driving the large pass transistor, is not enough and the system will act as an oscillator. Also, extremely high gain opamp can generate unstable feedback poles as presented in the

root-locus analysis in subsubsection 4.4.1.

Improvements in the design would have been to insist using a single-stage rectifier since the single-stage rectifier has a superior PCE performance and the output DC voltage it achieves at low power would have been enough to work with the LDO. The PCE performance could be estimated to be atleast 10% superior compared to the two-stage rectifier. The estimation is based on the simulations results using ideal components. In the reference circuitry, the temperature behaviour dependence could have been taken into account as the typical PTAT (current) and CTAT (voltage) behaviours affect the operating point of the LDO, even though the circuit was designed to work in a constant temperature environment. In overall, the reference circuitry is the weakest point of the system as it limits the LDO operation range to 1.4V. Too much emphasis was placed on power consumption and instead an output buffer along with temperature compensation should have been added, so that the BMR operational amplifier range could have been maximized.

For future designs: A folded-cascode opamp is theoretically a good candidate for error amplifier, as it provides good capacitive driving with two-stage opamp gain and single-stage opamp zero-pole behaviour. Folded-cascode opamps have been implemented in LDO's in [13] and [30].

The objectives of the work presented in this thesis were low power consumption, full-bandwidth regulation power system for biosignal measurement application in the UHF RF-band. During the work, the theory of designed circuits was thoroughly studied and applied to the practical realm. The operation of the developed circuits was verified with pre- and post-layout simulations indicated sufficiently good performance for the intended purpose.

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